LeCroy

Quad 10-Bit Transient Digitizer

Model 8210

Revised

March 8, 1983

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A T T E N T I O N

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS,AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

A T T E N T I O N

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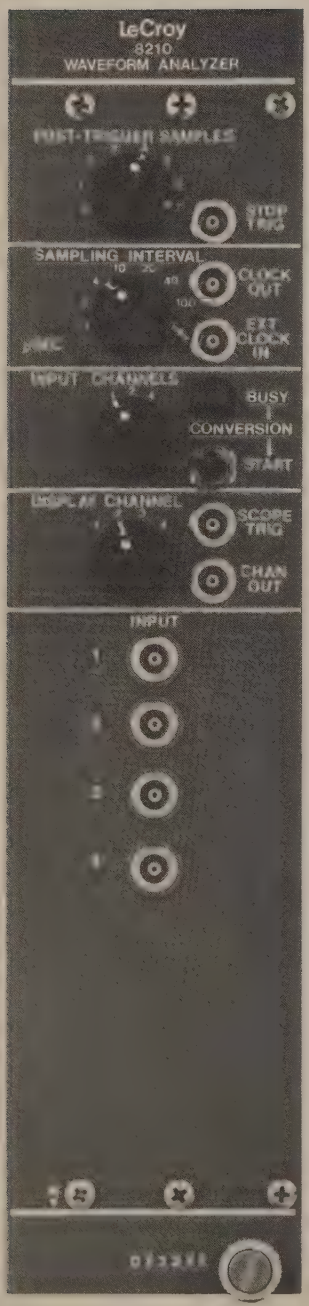
TECHNICAL DATA

LeCroy



Quad 10-Bit Transient Digitizer

Model 8210

- **4 Analog inputs**
- **10-bit resolution**
- **10mV/count sensitivity**
- **±100 psec aperture uncertainty**
- **Simultaneous sampling (<5 nsec uncertainty)**
- **5 MHz analog bandwidth**
- **Front-panel post-trigger sample select**
- **Large scale expandable memory of 32K words/module**
- **Protected inputs**
- **Built-in display driver**
- **System compatibility—part of a LeCroy digitizer family**
- **Varying clock rates possible**

The LeCroy Model 8210 Quad 10-Bit Transient Digitizer is part of an expanding line of LeCroy products for the study of transient phenomena. The 8210 offers the user a medium speed, high performance, modular waveform digitizer designed in accordance with CAMAC standards, providing high data transfer rates and system flexibility. Up to 4 analog inputs to the 8210 are sampled simultaneously by track-and-hold circuits having analog bandwidths greater than 5 MHz and channel-to-channel sampling uncertainty of <5 nsec. The analog signal is digitized by a 10-bit, successive approximation ADC. The data is stored in the Model 8800/10 memory module under the control of the 8210. Each 8800/10 module has a capacity of 32K, 10-bit words; up to 8 memory modules may be used in a serial fashion. The memory per channel is the total memory divided by the number of active channels. (Further expansion possible as factory option.)

The data is read out through the memory control circuitry in the Model 8210. Each of the four channels can be separately addressed. Readout is non-destructive, and a DAC display is provided for presentation on any scope.

The flexibility of the design concept also allows the external clock frequency to be varied with time, permitting "importance" sampling along a single waveform. LeCroy's CAMAC Model 8501 Programmable Three-speed Clock Generator provides a wide range of clocking capabilities including "importance" sampling under CAMAC control.

The flexibility of 8210 may be enhanced through the use of the Model 8100 Dual Programmable Differential Amplifier. This module affords excellent common mode rejection and offers a wide range of CAMAC-programmable gain.

The 8210 system digitizes continuously, which allows retention of waveform data recorded before the stop trigger. This pretrigger sampling capability allows recording the baseline value previous to the occurrence of the meaningful signal or allows triggering from a feature of the signal while retaining previous detail.

The Model 8210 is packaged in a #3 width CAMAC module. All integrated circuits are socketed, and boards are hinged for easy maintenance.

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Innovators in Instrumentation

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SPECIFICATIONS
CAMAC Model 8210
QUAD 10-BIT TRANSIENT DIGITIZER

Input Characteristics:

Number of Inputs:	1, 2 or 4, switch selectable.
Analog Input Impedance:	1 MΩ (50 Ω optional).
Full-Scale Amplitude Range:	±5 volts—10 volt range.
Input Analog 3 dB Bandwidth:	5 MHz.
Overvoltage Protection:	± 65VDC, ± 100V for 1sec, ± 200V for 10msec.
Stop Trigger Input:	LEMO connector, TTL level required to terminate conversion cycle after preset number of samples.
Input Connectors:	Coaxial LEMO.
Input Coupling:	Direct.

Digitizing Sections:

Internal Clock:	Front-panel switch selects rate: 1 MHz, 500 KHz, 250 KHz, 100 KHz, 50 KHz, 25 KHz, and 10 KHz, or EXT.
External Clock Input:	One coaxial LEMO-type connector (500Ω impedance, TTL level). Minimum duration of clock pulses, 100 nsec. Valid frequency range 0 to 1 MHz. Time varying frequencies allowed to achieve "importance" sampling along a single waveform.
Sensitivity:	9.8 mV/count.
Analog-to-Digital Conversion:	10 bits or 1 part in 1024.
Linearity:	±0.2% of full scale.
Aperture Uncertainty:	±100 psec maximum, defined as the uncertainty in the actual sample-taking time relative to the leading edge of the clock. This corresponds to a capability of frequency reconstruction of 1.5 MHz with 10-bit accuracy.
Channel-to-Channel Sampling Uncertainty:	≤ 5 nsec.
Memory Organization:	The memory is contained in separate modules which can be cascaded each capable of storing up to 32,768 10-bit words. (See further description of LeCroy Model 8800). Memory is divided equally among the active channels.
Display:	A built-in display driver allows the digitized waveform to be viewed on any real time oscilloscope. A channel select switch is located on the front panel.
Post Trigger Sampling:	The number of samples taken after the stop trigger is set by a front panel switch in multiples of 1K (2K optional).

Readout Characteristics:

Readout Scheme:	The standard CAMAC organization is used permitting readout at the maximum rate allowed by CAMAC unless 4 channels are active (2μsec/word). Word count and Q-switching DMA transfers are possible. Readout is non-destructive. Data from individual channels is accessible and the first word corresponds to the earliest sample taken. Readout is serial, but readout can be terminated for a given channel at any point.
CAMAC Commands:	L: A Look-At-Me signal is generated at the end of the final sampling sequence. Q: A Q=1 response is generated in recognition of a F(2)•N only when a valid word is being read. After all data has been read for a given input channel, the next readout will generate a Q=0 response. The size of the memory, which depends upon the number of memory modules used, is programmed into the 8210 by a jumper option. Q=1 also returned on F(8) if internal LAM is on. Z: The continuous sampling cycle is reinitiated; requires S2. C: Same effect as Z. X: An X=1 (Command Accepted) response is generated when a valid F and N are generated.
CAMAC Function Codes:	F(1): Reads out front-panel switches (number of post-trigger samples, number of channels and internal clock frequency). F(2): Read data registers; requires N. Successive F(2)•N commands will read successive 10-bit words from memory. F(8): Test for LAM. F(9): Initialize module. F(10): Clear LAM. F(16): Select channel to be read. F(16)•A(0) through A(3) selects channel 1–4 of the quad unit. F(24): Disable Look-At-Me (LAM): requires N • S2. F(25): Generates a "Stop Trigger." F(26): Enable LAM and stop DAC display. This command is necessary for any computer readout of the module. There may be as much as a 20 msec latency period (for 1 memory module) to allow the DAC to cycle through the rest of memory. (Caution: the state of the LAM mask, and hence the state of the display, may be arbitrary after turn-on.) No latency time if issued before stop trigger.
Packaging:	In conformation with the CAMAC standard for nuclear instrumentation modules. (IEEE Standard 583, or European Esone Report #EUR4100e.) RF shielded CAMAC #3 module. Approximate current requirements are within CAMAC standards for a #3 width.
Power Requirements:	+6V at 2.2A −6V at 13mA +24V at 490mA −24V at 310mA

SPECIFICATIONS SUBJECT TO CHANGE

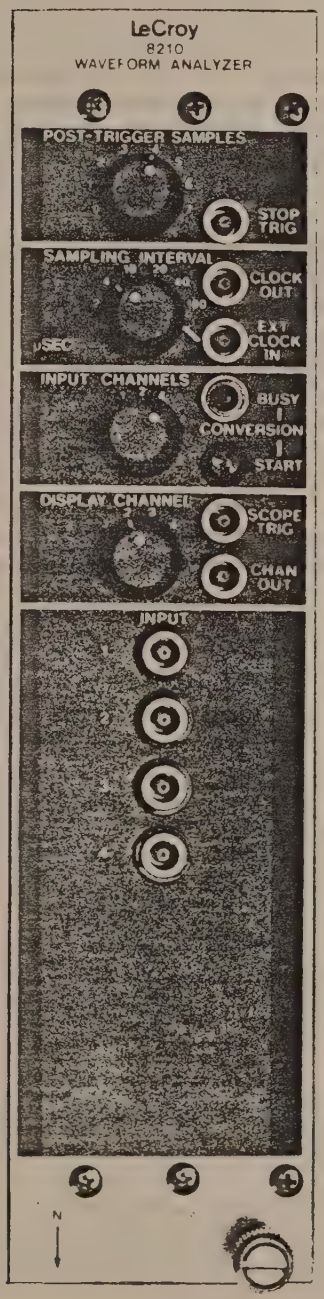
Front Panel Photograph and Description

Switch selects number of samples taken after the stop trigger.

Switch selects number of microseconds between samples.

Switch select number of input channels and determines highest possible frequence.

Switch selects channel to be displayed.



TTL level pulse initiates post trigger run down scaler.

Drives 50 ohm load to TTL level at the internal clock sampling rate

Leading edge of TTL pulse causes unit to take a sample in all channels.

LED lights when unit is digitizing.

Manual pushbutton initiates sampling.

Separate scope trigger allows manipulating of scope gain, time base, etc. without losing trigger.

Display output proportional to input signal at a flicker free refresh rate.

Individual Inputs 1 megohm impedance in the H option.

3. ADDENDA TO SPECIFICATIONS

Memory Organization:	The memory is contained in separate modules, each capable of storing up to 32,768 12-bit words.....
Display:	.....Each sweep consists of a separate positive sync signal for trigger purposes and a waveform proportional to the amplitude of the input signal. .....
Current Requirement:	+6 volts at 2.2A -6 volts at 13ma +24 volts at 490ma -24 volts at 310ma

4. OPERATIONAL DESCRIPTION

General

The LeCroy Model 8210 Multichannel Waveform Digitizer is a 10 bit (.1% resolution) analog to digital converter which can process signals from four different sources simultaneously. The maximum sampling rate is 1MHz for each channel. Data is stored in an external 32K word memory module which divides memory size equally among the input channels. The memory can be expanded to 3,32K word modules.

The A/D conversion for each sample is effected by an independent sample and hold and ADC for each channel. Data is converted within 1μsec independent of the master clock frequency. The digital data is then directed by internal circuitry to the 8210 output connector along with timing and control signals appropriate for interfacing with LeCroy Model 8800/10 cascadable memory modules. This allows the data to be stored in a memory of up to 96K, 10 bit words, in 32K increments.

The Model 8210 also contains circuitry which sequentially reads the memory and sorts the data such that the digital data for any selected channel can be placed on the CAMAC dataway or reconverted to analog form by an internal DAC for viewing on an external scope.

Front Panel Inputs, Controls and Indicators

Analog Inputs: Four LEMO type input connectors. Input impedance 1M Ω, bandwidth greater than 5MHz. Full scale amplitude range is ±5.00 volts, ±1% of F.S.

Sampling Period Switch: The sampling period per channel may be internally set to the rates indicated at the first seven positions of the switch; 1, 2, 4, 10, 20, 40 and 100 μsec. When the switch is in the Ext. Clk. position, the sampling period is determined by the frequency of the external clock.

External Clock Input: Allows user to determine sampling rate per channel by input from a TTL level clock generator. Input Impedance is 50 Ω. The maximum allowable external clock frequency is 1MHz (also applies to internally selected clock rates). Conversion is initiated on the positive edge of the clock.

To allow for "importance sampling", the clock rate may vary over the allowable range provided the clock is free of anamalous trailing edges.

No. of Input Channels Switch: Programs digital multiplexer to select data from channel one only in the 1 position, from channels one and two only in the 2 position and from channels one through four in the 4 position.

Conversion Start Button: Resets internal logic and starts countinuous sample, convert, and store cycling. This button must be pushed after changing the "No. of Input Channels" switch.

Busy Indicator: LED adjacent to conversion start button lights during sample, convert and store operations, remains off during readout and display operations.

Stop Trigger Input: LEMO type connector, 500 Ω input impedance, requires positive going TTL pulse of at least 50 nsec duration. A proper trigger will stop the data conversion and storage process after the selected number of post-trigger samples have been taken.

Post-Trigger Samples Switch: The position of this switch controls the number of samples converted and stored per input channel following the stop trigger pulse. The switch has positions 0 through 7. Normally the unit is programmed (wire jumpers) such that the numbers correspond to thousands of post-trigger samples, i.e., position 7 means 7K post-trigger samples per channel. The programming of the switch is done on a wire jumper platform. (See appendix A for jumper options).

Display Channel Switch: Digital data of selected channel is reconverted to an analog signal for display on a scope. The signal is available from the "channel out" connector.

*NOTE: During operation the display channel switch and post-trigger samples switch may be changed at any time but the other panel switches should be preset before a conversion is initiated and not changed until a new conversion-readout cycle is to be initiated under new conditions. The internal timing may be upset by changing these switches so that the logic must be reset by starting a new conversion cycle to restore the proper timing as determined by the settings of the switches.

Front Panel Outputs

Internal Clock Out: Drive 50 Ω load to TTL levels. Permits synchronization of multiple 8210's by timing all sampling with respect to a single clock.

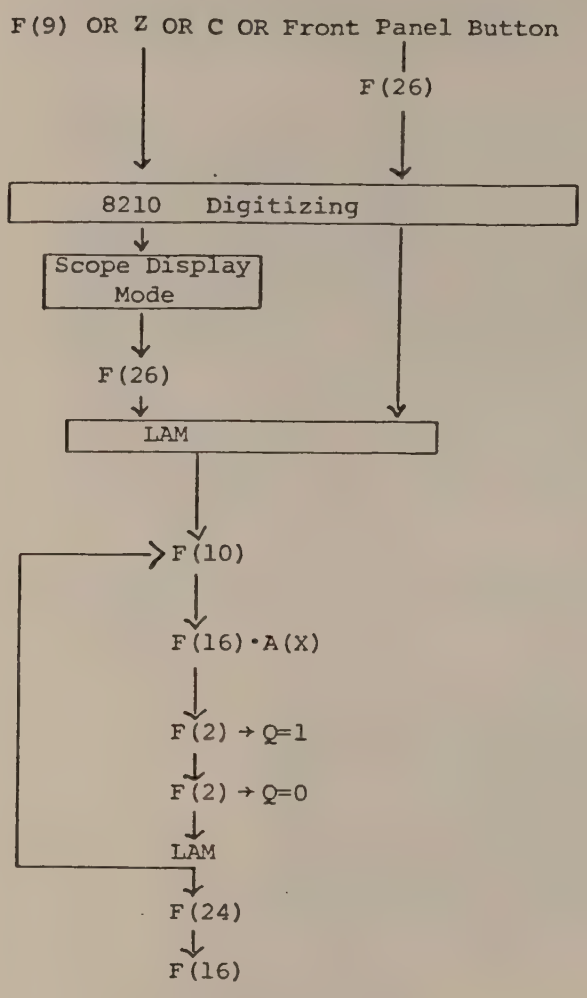
Channel Display Output: LEMO connector. After a stop-trigger and the selected number of post-trigger samples per channel has been digitized the Model 8210 will enter the scope display output mode (unless the LAM is enabled - see CAMAC section). The data from any input channel may be displayed on an oscilloscope by setting the display channel switch to the desired channel number. The amplitude of the output signal into a high impedance scope input is between 0 volts and +10 volts (the scope display output should not be terminated). The data points are displayed at an

approximate rate of 1.5 µsec per point in the one channel mode, 3 µsec per point in the two channel mode, and 6 µsec per point in the four channel mode. The scope sweep rate is set by the user to display the desired number of points.

Scope Trigger OUT: LEMO Connector. A TTL positive going pulse occurring at the time the first data word is output for display. This pulse may drive the external trigger input of a scope so that the sweep will always start with the earliest data point. This output should not be terminated.

Jumper Platform: The 8210 digital board contains a jumper platform (socket 3L) which in conjunction with the front panel "Post-Trigger Samples" switch programs the number of post-trigger samples. It also programs the number of 8800 memory modules (max. 3) to be used.

EXAMPLE OF 8210 CAMAC CONTROL SEQUENCE



F(9) OR Z OR C OR Front Panel Button – Initiate Sampling

F(26) — Enable LAM (only necessary if 8210 is to enter CAMAC readout mode after conversion completed).

8210 Digitizing — Stop Trigger pulse OR F(25)

Scope Display Mode — 8210 enters scope display mode unless F(26) command was performed above.

F(26)

LAM — 8210 ready for CAMAC readout (Read LAM or test for LAM by Q=1 in response to F(8)).

F(10) — Reset LAM

F(16)·A(X) — Select channel for readout (see Table I)

F(2) → Q=1 — READ DATA for selected channel.

F(2) → Q=0 — Readout complete

LAM

F(24) — Disable LAM

F(16) — Enable scope display.

NOTE: All CAMAC F(X) commands require N.

SELECTING CHANNELS FOR CAMAC READOUT

TABLE I

CAMAC Command	No. of Channels Selected On Front Panel	Result
F(16)·A(0)	1	Select Channel number 1
F(16)·A(0)	1,2, or 4	Select Channel number 1
F(16)·A(1)	1,2, or 4	Select Channel number 2
F(16)·A(2)	4	Select Channel number 3
F(16)·A(3)	4	Select Channel number 4

*NOTE: a) F(16) commands also require N, S1 and S2. DATA is output in a offset binary code, i.e., the most positive voltage (+5. volts) is represented by all "ones", and the most negative voltage (-5. volts) by all "zeros".

b) The least significant bit is always on R1 and the most significant bit on R10

TABLE II

A) N·F(1) reads the setting of the post-trigger samples switch, the sampling period switch, number of channels switch and odd/even samples flag.

(a) Post-Trigger Samples Switch Setting	2^2 R3	2^1 R2	2^0 R1	(Code) (CAMAC R Lines)
7	0	0	0	
6	0	0	1	
5	0	1	0	
4	0	1	1	
3	1	0	0	
2	1	0	1	
1	1	1	0	
0	1	1	1	

(b) Sampling Period Switch Setting	2^2 R6	2^1 R5	2^0 R4
Ext.	0	0	0
100 µsec	1	0	0
40 µsec	0	1	0
20 µsec	0	1	1
10 µsec	1	0	0
4 µsec	1	0	1
2 µsec	1	1	0
1 µsec	1	1	1

(c) No. of Channels Switch Settings	2^1 R8	2^0 R7
4	1	1
2	0	1
1	0	0

(d) ODD/EVEN Flag - If running in the single channel mode, the 8210 will truncate the last sample if it is to be stored in the first half of the 8800 memory. This condition is flagged on R9 during N·F(1).

R9=0: No Sample Truncated - Earliest sample = 32K·(No. of 8800S) - Post Trigger samples from trigger.

R9=1: One Sample Truncated - Earliest sample = (32K·(No. of 8800S)+1) Post Trigger samples from trigger.

5. FUNCTIONAL DESCRIPTION

General

The Model 8210 is a multichannel waveform digitizer composed of analog to digital converter (ADC) boards and a controller board which contains digital circuits needed to control the storage of data in the Model 8800 memory modules. This board also contains the circuitry needed to read the data from the memory and either places the data on the CAMAC Dataway under CAMAC control or reconstructs the analog signal in any channel for display on a lab scope. Other circuitry on the board permits reading the settings of the front panel switches as a digital code on the CAMAC Dataway.

In the following functional description of the instrument the operation of the boards will be discussed separately, and each board will be divided in several logical subsections. A schematic of the controller and ADC boards are found at the end of this section to help clarify testing and to aid in trouble shooting and repair.

ADC Boards

The ADC boards for the 8210 are composed of a track and hold circuit followed by a 10 bit, successive approximation ADC. The ADC converts one sample in one microsecond. The track and hold timing is folded into the ADC timing to achieve a one megasample/sec throughput rate without degrading the high frequency performance of the system.

The digital data from the ADC is held in tri-state output latches after the conversion is completed. During the next sample the controller board sequentially scans these latches and stores the data in memory.

Controller Board

General description - refer to first paragraph in the functional description section.

Master CLK: The Master CLK pulses come from a digital multiplexer (74LS151) which multiplexes several gates of different frequencies from the outputs of a divider (74LS390) clocked by a 4 MHz crystal oscillator. An input from an external connector may also be selected by the multiplexer for external control of the sampling rate. The 74LS151 is programmed by the sampling rate switch on the front panel.

Memory Strobe and Refresh Generator: After data has been entered into the FIFO's (9403's) it bubbles through toward the FIFO output register. Status signals from the FIFO output and clock signals from a 5 MHz oscillator (74LS324) then control the shifting of the data out of the FIFO's onto the memory datalines in synch with memory strobe pulses. This control is accomplished by the memory strobe and refresh pulse generator logic. This logic generates refresh pulses about every 10 μsec and ensures that memory strobe pulses and refresh pulses do not overlap and are properly timed with respect to one another. (See Model 8800 manual for detailed timing diagrams).

Data Display/CAMAC Readout Control: This section controls the readout of the data from the FIFO's and selects the data words to be latched into the DAC input register and the tristate buffer registers which output to the CAMAC dataway. As soon as the first word flag and first data word appear at output registers of the FIFO's the internal logic is set up to begin readout. Readout may proceed in a continuous cyclic mode or in a interrupted single memory scan under control of CAMAC F(2) read commands depending on the state of the CAMAC ENABLE line. If this line is low the readout will be under control of the FIFO's and Readout control logic alone and will proceed automatically at a rate depending on FIFO timing and the timing of monostables inside the readout control section itself. A scope trigger pulse is initiated when the first word flag is up so that the display sweep may be triggered at the earliest sample in the data.

Selection of the channel to be displayed is done by: (1) the display channel switch and (2) the programmable sequencer made up of a 9319 (4J), a 74LS151 (5J), a 74426 (5K), a 74LS173 (5I), a 74LS74 (6H) and other logic gates. This circuitry decides at the beginning of a read cycle how many data words are skipped before a latch pulse is sent to the output registers. It does this on the basis of input data from the 2^1 and 2^0 terminals of the "Display Channel" switch on CAMAC A1, A2 information latched into the 74LS173 by an F(16)·S2 command when CAMAC controlled readout is to be done. After this initial positioning of the first latch pulse at the first word of the channel to be displayed, the circuitry decides how many words are to be skipped before another latch pulse is produced. It does this on the basis of input from the "Input Channels" switch. For example, in the single channel mode no words skipped, in the two channel mode one word is skipped and in the four channel mode two words are skipped between latch pulses.

When the CAMAC ENABLE line is set high by an F(26) command, a LAM will be raised when the first word flag and first word appears at the FIFO output registers. Now an F(16)·S1 pulse latches A1, A2 information in the 74LS173 to determine which channel is to be read (see previous paragraph). F(16)·S2 starts the normal readout process discussed before and the first dataword is latched into the output latches and readout proceeds until the next word from the selected channel appears. No latch pulse is produced and readout

stops until the first word has been placed on the CAMAC data lines by an F(2) command which enables the register output. The next word is then latched into the register on the trailing edge of the F(2)·S2 pulse and readout proceeds until the next word appears at the register inputs but again halts until another F(2)·S2 releases the previous word to the dataway and then latches this next word into the register and restarts the readout. Readout proceeds in this fashion until the first word flag and the accompanying data word appear again, at which time readout stops until another F(16) is received. If an F(24) command is issued the CAMAC ENABLE line goes low, the LAM is disabled and the F(16) command will reset the logic into the data display mode.

CAMAC Control Logic: This section uses 74LS164(5A) and some other logic gates to decode the CAMAC function lines and generate the CAMAC control and response signals. For a complete description of these commands and responses see the CAMAC command and function code section of the data sheet and the CAMAC command sequence on page 4.3 .

Memory Enable Control: This circuitry is included on chips located in sockets 5M (½74L279) and 2C (½74S08). The initiate pulse sets the Memory Enable line low enabling the first memory in the chain connected to the 8210. The line returns high when the first memory strobe pulse occurs (enabling is done by high to low transition). When the last memory is full a memory enable return pulse is sent back to the controller and causes the memory enable line to go low reenabling the first memory again. For more details see the Model 8800 manual.

Auxiliary and Monitoring Circuitry: Allows digital codes associated with each front panel switch (except "display channel" switch) to be gated onto the CAMAC dataway by appropriate CAMAC commands through tristate buffers (74LS 240A) located in socket 3K.

A 7485(4K) monitors the "display channel" switch and "input channels" switch and disables the display DAC if the "display channel" switch is set to a channel which does not have its input switched into the multiplexer as determined by the setting of the "Input Channels" switch.

CONTROL SEQUENCING

(Refer to diagram on Page 4.3)

Initiate Sampling: The 8210 will start sampling after depressing the front panel pushbutton or by computer command of a Z, C or F(9). The unit will remain in the sampling mode, continually cycling through memory until detecting a stop trigger.

Stop Sampling: After detecting a stop trigger (either using the external TTL pulse or CAMAC F(25) the 8210 will execute the required number of post-trigger samples (as determined by the front panel switch) and then enter the readout mode. The user should not apply a stoptrigger until the 8210 has cycled completely through memory after "initiate sampling"; otherwise the memory will contain old and new data. The time required to cycle through memory once is given by:

$$Tcycle = 32768 \cdot \frac{NOM}{NOC} \cdot T_S$$

Tcycle = cycle time through memory in seconds
NIM = number of 8800 memory modules
NOC = number of channels (1, 2, 4)
T_S = sampling time (front panel switch or external) in seconds.

Readout:

1) After entering the readout mode the 8210 will either display data on the scope or await CAMAC readout commands. If the user issued a F(26) command before the stop trigger the unit will automatically enter the CAMAC readout mode. If F(26) was not issued then the unit will display data on the scope display until F(26) is issued.

2) When the 8210 is ready to begin CAMAC readout it will turn the LAM on. The user can detect this by enabling interrupts or issuing F(8) commands and testing for Q=1. Upon detecting the LAM (or Q=1 on F(8)) the user should execute a F(10) command to clear the LAM. If the LAM is not cleared the unit will not read data from another channel later in the control sequence (step 6).

3) The user now selects which channel he wants to read by executing the appropriate F(16)·A(X) command (see Table I)

4) Data is read by issuing successive F(2) commands. The data is read as offset binary (see Table I). Data can be read in one of two modes:

   a) Block Transfer - The number of F(2)'s issued equals the number of words to be read.*

   b) Q Transfer - User executes F(2) until Q=0 is detected. Issuing F(2) after all data is read* does not affect the 8210.

5) The maximum readout speed is:

   a) 1 MHz in the 1 channel mode

   b) 500 KHz in the 2 channel mode

   c) 250 KHz in the 4 channel mode

   Exceeding the maximum readout speed will result in a Q=0 response on F(2).

6) Once all data has been read from the selected channel the LAM is set again. To read another channel execute the same steps from 2) on. To reenable the scope display the user must issue a F(24) followed by F(16)·A(0).

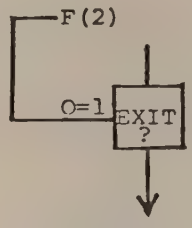
7) Since the 8210 serially reads <u>all</u> memory during readout it is not possible to stop readout before detecting Q=0 on F(2) (or total block transfer) and then reading another channel.

*<u>NOTE</u>: The amount of memory allocated to each channel depends on the number of channels selected and the number of 8800 memory modules:

Memory/Channel = 32768·NOM/NOC
NOM = number of 8800 memory modules
NOC = number of channels (1, 2, 4, 8)

SHORT CYCLE READ SEQUENCE FOR 8210

If user does not want to read all data from a selected channel he can "short cycle" the unit at any time by executing a F(24) followed by a F(2).



User performs F(2)

F(24)

User decides to read another channel before reading all data from the selected channel

F(2)

One more F(2) needed to put unit back in scope display mode

8210 or 2264 now displaying on scope

F(26)

User decides to read next channel

LAM

Sequence is now the same as in the manuals for selecting and reading channels

OPERATIONS SECTION MODEL 8210

INTRODUCTION

This manual is not written as a basic trouble-shooting guide but rather as a detailed operational description of the 8210 circuits. It is assumed that the reader is familiar with the basic operation of the 8210 and understands digital/analog circuitry.

ADC BOARD

The 8210 contains two identical ADC boards, each of which contains two track and hold circuits, two analog-to-digital converters, and logic to provide control and output buffering. Circuitry on the board can be separated into two major blocks; 1) the track and hold circuits and 2) the A/D converter & controls section.

TRACK AND HOLD CIRCUITS

As shown in the block diagram in Fig. A, the track and hold circuit is a conventional open-loop circuit made up of an input buffer amplifier, switch, storage capacitor and output buffer amplifier, plus feedthrough & pedestal cancellation circuits.

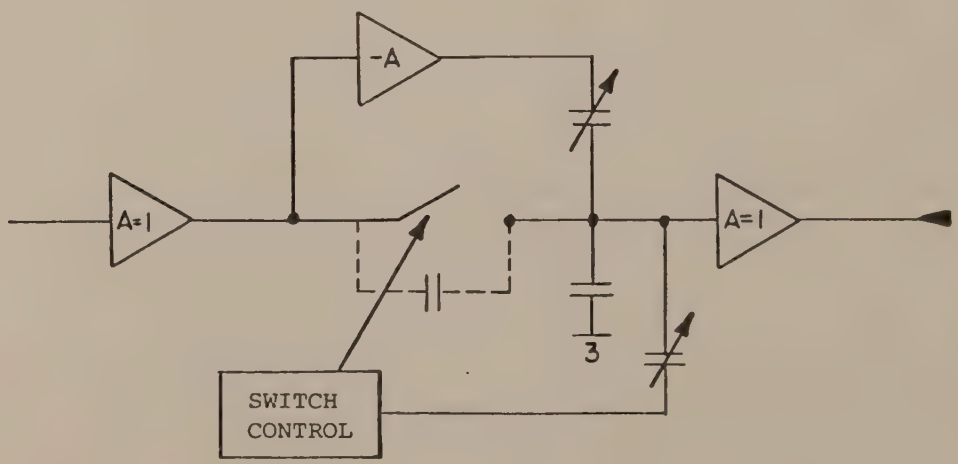


FIG. A

Both channels on the board have identical circuits, so only one will be described.

The input buffer is shown in Fig. B. Q1 is a matched pair of N-channel junction FETs connected to form a "zero offset" source follower, with the lower FET, CR5 and R6 acting as a current source and the upper FET providing the signal path. The voltage drop across R2 compensates for the voltage drop across R6. CR5 provides an additional drop to compensate for the emitter-base voltage of Q2, giving the buffer amplifier a very low DC offset: R6 permits adjustment of that offset.

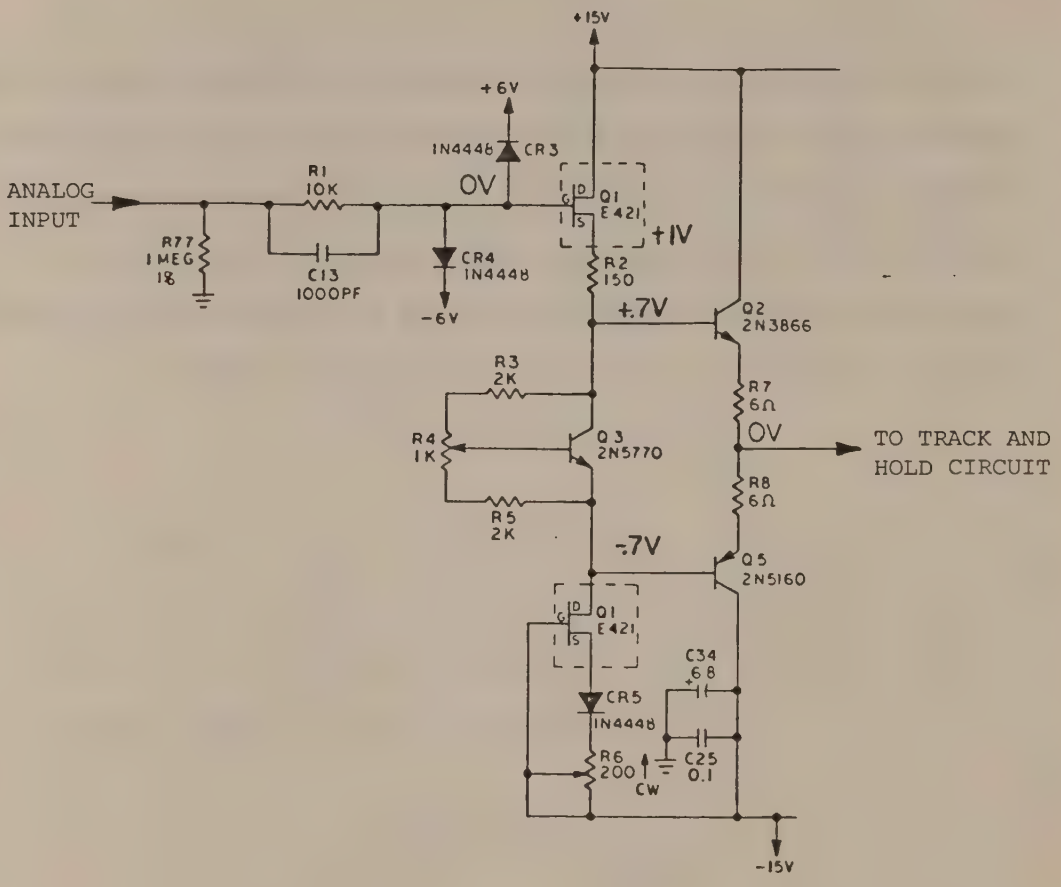


FIG. B

TRACK AND HOLD INPUT BUFFER

Q2, Q3, and Q5 form a class AB power driver to provide slewing currents to the sample capacitor. Q3 generates a voltage drop that turns Q2 and Q5 on. R4 adjusts the bias current through Q2 and Q5 by setting the voltage drop across Q3. R77 sets the input impedance of the buffer, and R1, C13, CR3, and CR4 are an input overvoltage protection network.

The track and hold itself (see Fig. C) is made up of Q7, an N-channel MOS FET, which functions as the analog switch, and C17, the signal storage capacitor. Gate drive for the FET is provided by differential pair Q12 and Q13, which also provide level translation for the TTL $\overline{\text{HOLD}}$ command signal appearing at the junction of R30, R26, and C18. Q11 provides emitter bias current for Q12 and Q13; OP Amp 7A (output pin 7) assures temperature stability for that current. 7A (output pin 1) sets the switching threshold voltage for Q12 and Q13. R27, together with the emitter bias current provided by Q11, sets the gate drive amplitude. Pedestal cancellation is achieved by feeding the inverted gate drive signal to C17 through C16, thus cancelling the effects of gate-drain capacitance in Q7.

Q9 and Q10 provide an OFF reference voltage to Q7. This reference follows the analog signal to allow full gate signal amplitude without overdrive. This is necessary because of the relatively large input analog signal swing ($\pm$ 5V). Q9 and Q10 form an emitter-coupled gate, ensuring that the OFF voltage for the gate drive will be either the output voltage (via Q10) or the input voltage (via Q9 and Q6), which-

ever is more negative. CR8 and CR9 prevent emitter-base breakdown in Q9 and Q10; R21 provides a minimum bias current to the pair.

Source-to-drain feedthrough is cancelled by inverting the input signal via Q6 and summing it into C17 through variable capacitor C14. The signal at the junction of CR8 and CR9 is slso inverted via Q8 and summed to C17 through C15 to reduce feedthrough from Q7's gate. CR6 and CR10-12 are used for DC level shifting.

The output buffer stage (Fig. D) is identical to the input buffer, except that it does not contain the input protection and impedance-setting circuitry. It provides a very high impedance discharge path to the hold capacitor, and has a low output impedance to drive the A/D converter.

A good way to do DC adjustments on the circuit or to troubleshoot failure is to remove 3C, which disconnects both track and hold circuits from the logic portion of the board and switches both T & H circuits to "Track" mode. In this situation, the voltages marked on Figures B-D should apply (assuming no input signal).

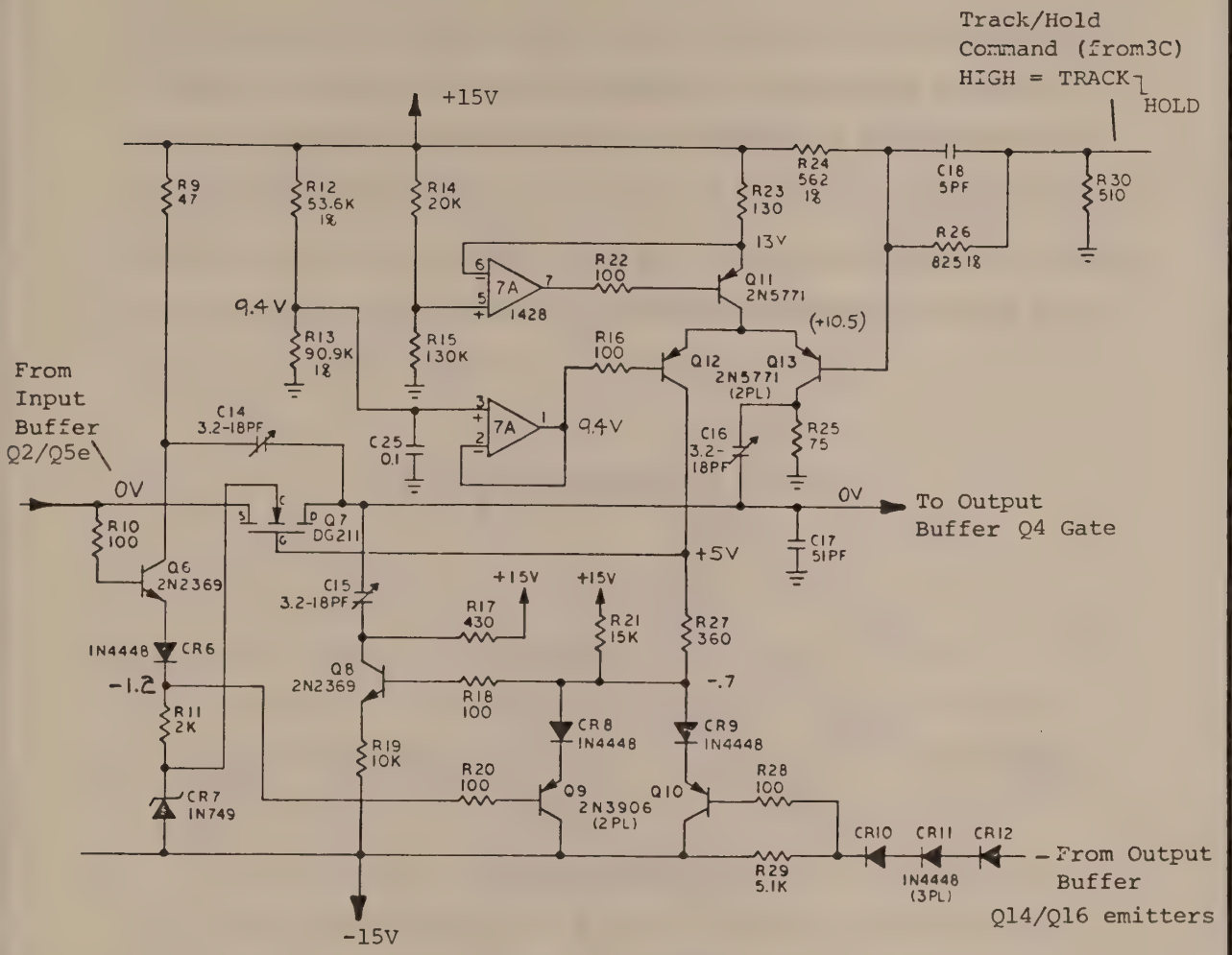
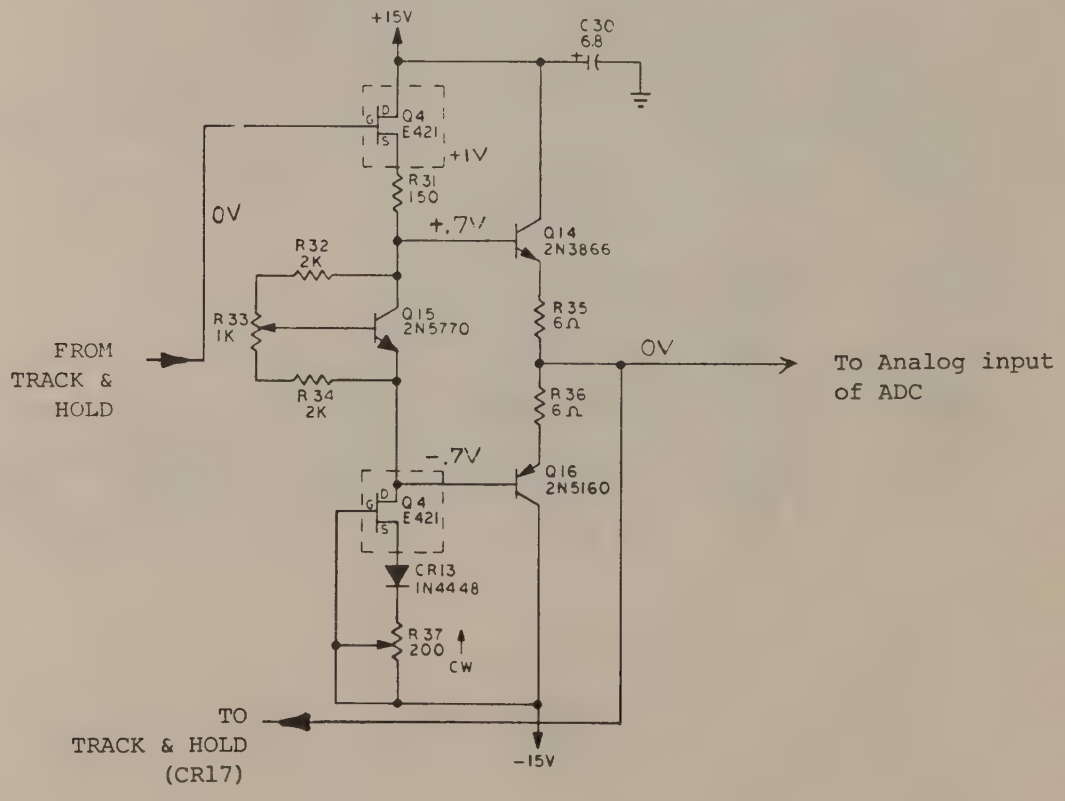


FIG. C

TRACK AND HOLD

Like most analog circuits, this one has many failure modes, and it's beyond the scope of this manual to detail them all. It may be worth mentioning one symptom as a starting point, however. If with 3C removed, the output of this circuit becomes fixed at a positive DC voltage, and will return to zero if an oscilloscope probe is touched to C17, then Q7 is not being turned on.



CR12,11 and 10 (Q10b)

FIG. D

TRACK AND HOLD OUTPUT BUFFER

If the gate drive voltage is at 5.5V, the FET is probably faulty; if not, the gate drive circuitry should be investigated.

One note of caution: if parts are replaced in either the input or the output buffer circuits, the output stage bias current adjustment pot for the relevant buffer (R4 in the input buffer stage, for example) should be set full clockwise to prevent overheating the output transistors. Follow the procedure in the alignment section.

A/D CONVERTER AND DIGITAL CONTROLS

The A/D converter used on the 8210 is a modular successive approximation type; i.e. during the conversion cycle, it makes 10 "tests", one for each bit starting with the most significant bit, to arrive at the output word. An output clock from the converter shows when each bit is being clocked into the converter output register.

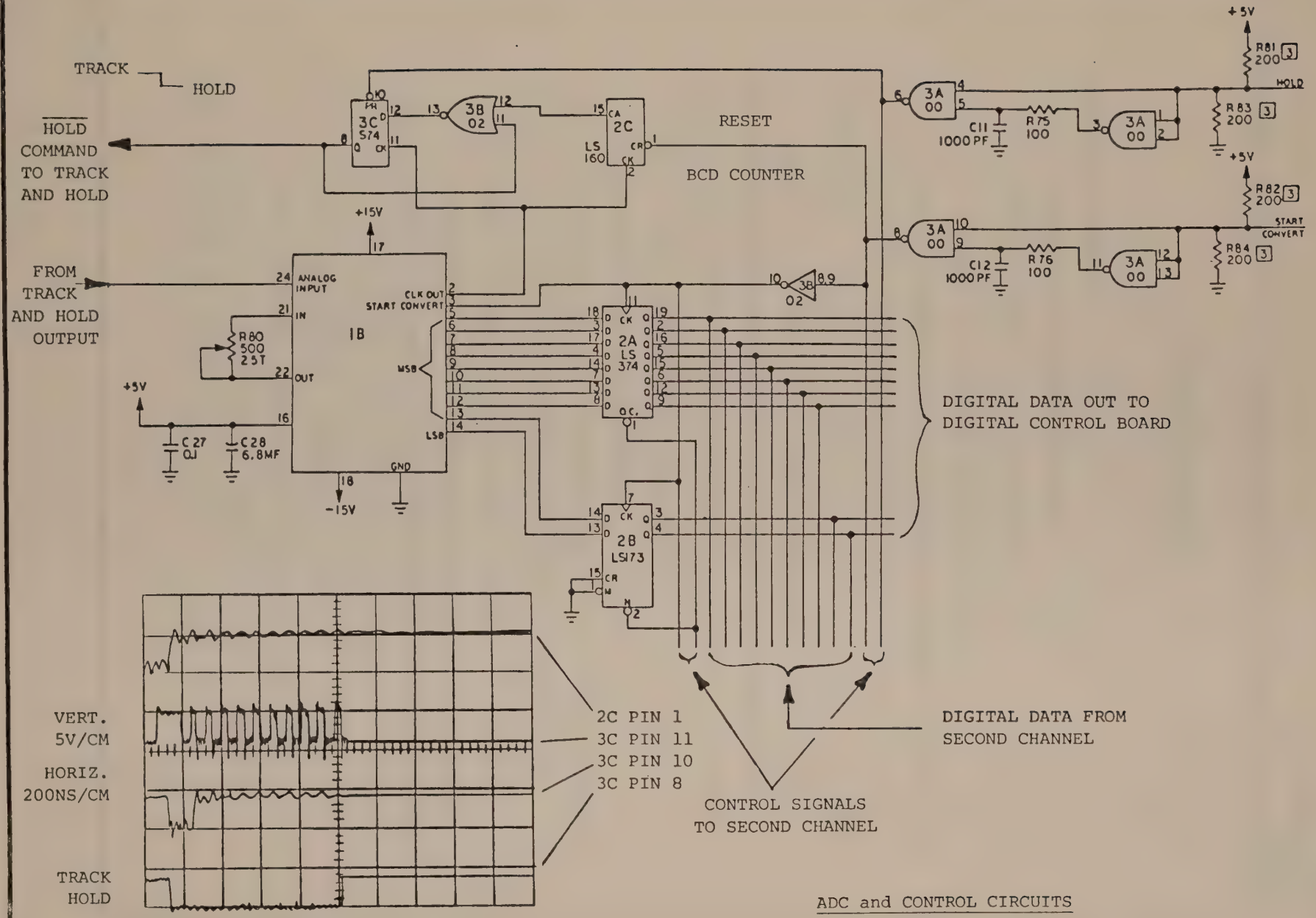
The 8210 makes use of this clock to switch the track and hold circuit to "Track" mode as soon as the converter has clocked out its last bit (Refer to Fig. E). BCD counter 2C is reset at the beginning of a conversion, and counts each of the converter's decisions, using the converter's cycle clock (2C pin 2). 2C reaches overflow one count before the conversion is complete (2C-15 high) and 3C pin 8 goes high on the next clock pulse (See timing diagram, Fig. E). 3B-13 assures that 3C-8 does not change state early in the cycle, since the Hold command does not come until slightly after the convert command is

given. 3C-8 is switched to the HOLD position (3C-8 high) by a command pulse at 3C pin 10. 2A and 2B are registers which hold the A/D converter's output word until the memory can accept it. They are clocked by the convert command pulse and their outputs are enabled (2B-2 & 2A-1) by commands from the control board.

The HOLD and CONVERT command signals are common to both channels on the board, and are derived from signals that come from the digital control board. The digital board's signals are formed into 100ns wide pulses by gate 3A and delay networks C11-R75 and C12-R76.

The other channel on the board is identical to the one described.

Both the Track and Hold circuit and the A/D converter use $\pm$15V supplies, which are derived on the board from the $\pm$24V CAMAC lines by two 1C regulators, 5A (-15v) and 6A (+15v).



ADC TIMING DIAGRAM

ADC and CONTROL CIRCUITS

Figure E

ALIGNMENT PROCEDURES

EQUIPMENT REQUIRED:

1. Oscilloscope with 15MHZ bandwidth.
2. Digital voltmeter with isolated inputs.
3. DC voltage source capable of ±5V output range.
4. Means of reading out data (CAMAC tester, computer system, etc.).

INTRODUCTION

Since the two channels on the analog board are identical, the reference designations for the upper channel will be shown first, with the lower channel reference designation following in parenthesis. All four channels must be adjusted separately.

1) Track and Hold; DC Adjustments:

Preliminary: It is not necessary for the board to be connected to the unit for DC adjustments; all that is required is a source of power to the rear CAMAC connector. If the board remains in the unit, it should be swung out on its hinges to allow easy access to the adjustment potentrometers. Before turning the power on, remove the 74S74 in position 3C from its socket, and turn adjustment pots R4, R33, and R41 and R70 fully clockwise. Removing the I.C. forces both track and hold circuits into "track" mode. Turn on the power. Allow 5 minutes for the unit to warm up.

A) Output Drive Bias Adjust:

Connect an isolated DVM between the emitters of Q2 (Q19) and Q5 (Q20). Slowly adjust R4(R41) until the voltage reads 60mV. Wait a few minutes, then recheck and readjust, as the reading will increase as the transistors warm up.

Repeat the above procedures after connecting the meter between the emitter of Q14(Q30) and Q16(Q32), using R33 (R70) for adjustments.

B) DC Offset Adjust:

1) Short circuit the analog inputs to the circuit to ground. Connect the DVM leads between the junction of R7(R44) and R8(R45) and ground. Adjust R6(R43) until the DVM reads OV$\pm$5mV.

2) Reconnect the meter leads between the junction of R35(R73) and R36(R74) and ground, and adjust R37(R72) until the DVM reads OV$\pm$5mV.

NOTE: If B(2) adjustment cannot be made, and the offset is positive and large (1V) check to see if the gate of Q7(Q22) is at about +5V. If not, and the I.C. at 3C is removed, then the drive circuitry is faulty and should be repaired before proceeding. If so, Q7(Q22) may be faulty. This can be checked by clipping a short circuit between source and drain; if the offset

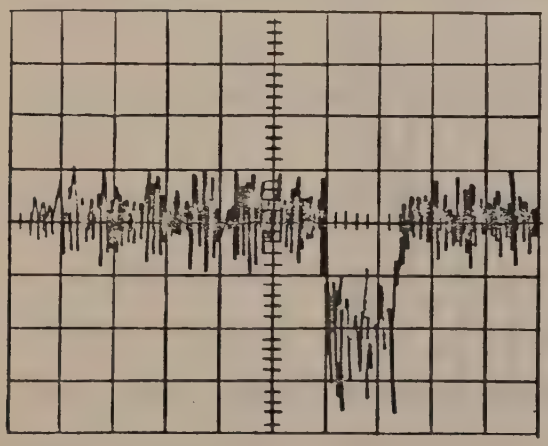
disappears, then the FET is faulty.

This completes the DC alignment of the track and hold.

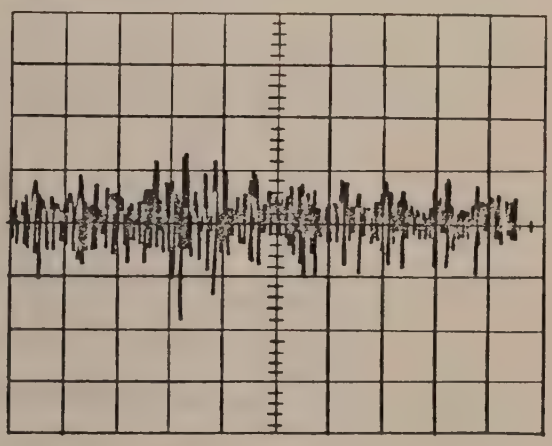
C) PEDESTAL ADJUSTMENT:

Turn off the power, replace 3C and reconnect the board to the instrument, using extender cables so that the board can be swung out for access to the adjustments. Set the unit internal clock for a 1 usec interval and turn on the power. Using the external synchronizing input on the oscilloscope, synchronize the oscilloscope to the 8210 clock output. Connect a scope probe to the junction of R35(R74) and adjust C16(C22) for minimum pedestal. See photographs below.

BEFORE ADJUSTMENT



AFTER ADJUSTMENT



VERT: 50mV/CM
HORIZ: 100nS/CM
(Same for both diagrams)

FIG. 1

D) DC Calibration:

Preliminary: For this and the next part of the procedure, the unit must be connected to the memory and to a computer system that can read out the memory and translate the digital data into a voltage readout (The computer readout is not necessary for the next section).

1) Connect a DC source to the analog input and adjust it to output +4.900 volts. Taking successive readings on the computer (sample rate 1 usec) adjust R33(R70) until the computer readout is +4.900 $\pm$ 10 mV.

2) Adjust the DC source to output -4.900V. Taking successive readings with the computer (sample rate still 1 usec) adjust R80(R79) until the computer readout is -4.900V $\pm$ 10mV.

3) Repeat #1 and #2 until no change in readout occurs.

This completes the DC calibration of the unit.

E) High Speed Adjustments:

Connect the "Channel Out" connector on the 8210 to the oscilloscope inputs. Connect "Scope Sync" output to the oscilloscopes' "External Trigger" input. Set scope input sensitivity to 2V/cm and trigger externally. Connect a sine wave generator to the appropriate input

channel, and adjust it to output a 10Vp-p sine wave at 500KHZ. Set the 8210 time base to 1 usec, the "Input Channels" switch to 4 and the "Channel Displayed" switch to the channel to be adjusted. To take a recording, press the reset button and, after a pause, input a TTL signal to the stop trig input (connecting the clock out to the stop trig works well here). Adjust scope time base to display entire channel memory (assuming only 1 memory module is connected to the unit). Carefully adjust the generator frequency, taking recordings after each adjustment, until the oscilloscope wave form looks like the photograph in Fig. 2.

SCOPE VERT.
-2V/CM
HORIZ.

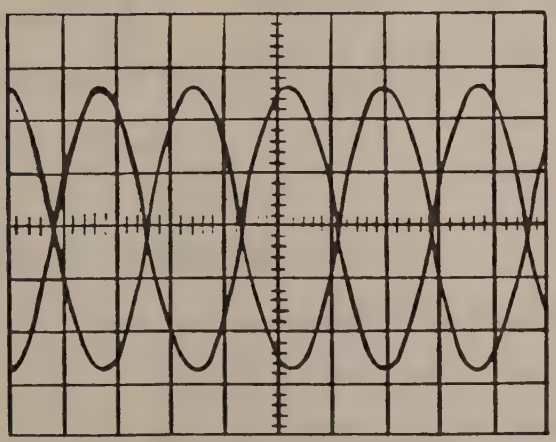
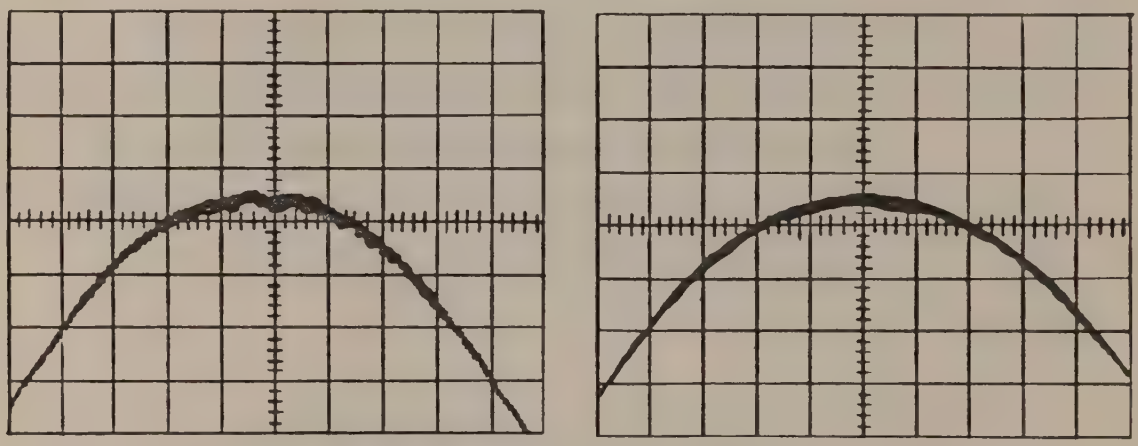


FIG. 2

Expand this wave form X10 horizontally and change the vertical sensitivity to .5V/CM. Examine the upper portion of the waveform. Adjust C14(C20) and C15(C21), taking a recording after each adjustment, until the waveform resembles the ones in Fig. 3b.

INCORRECT HIGH SPEED ADJUSTMENT

CORRECT HIGH SPEED ADJUSTMENT



NOTE:VERTICAL = 5V/CM (BOTH DIAGRAMS)

A.

B.

FIG. 3

This completes the alignment of the unit.

8210 - CONTROL

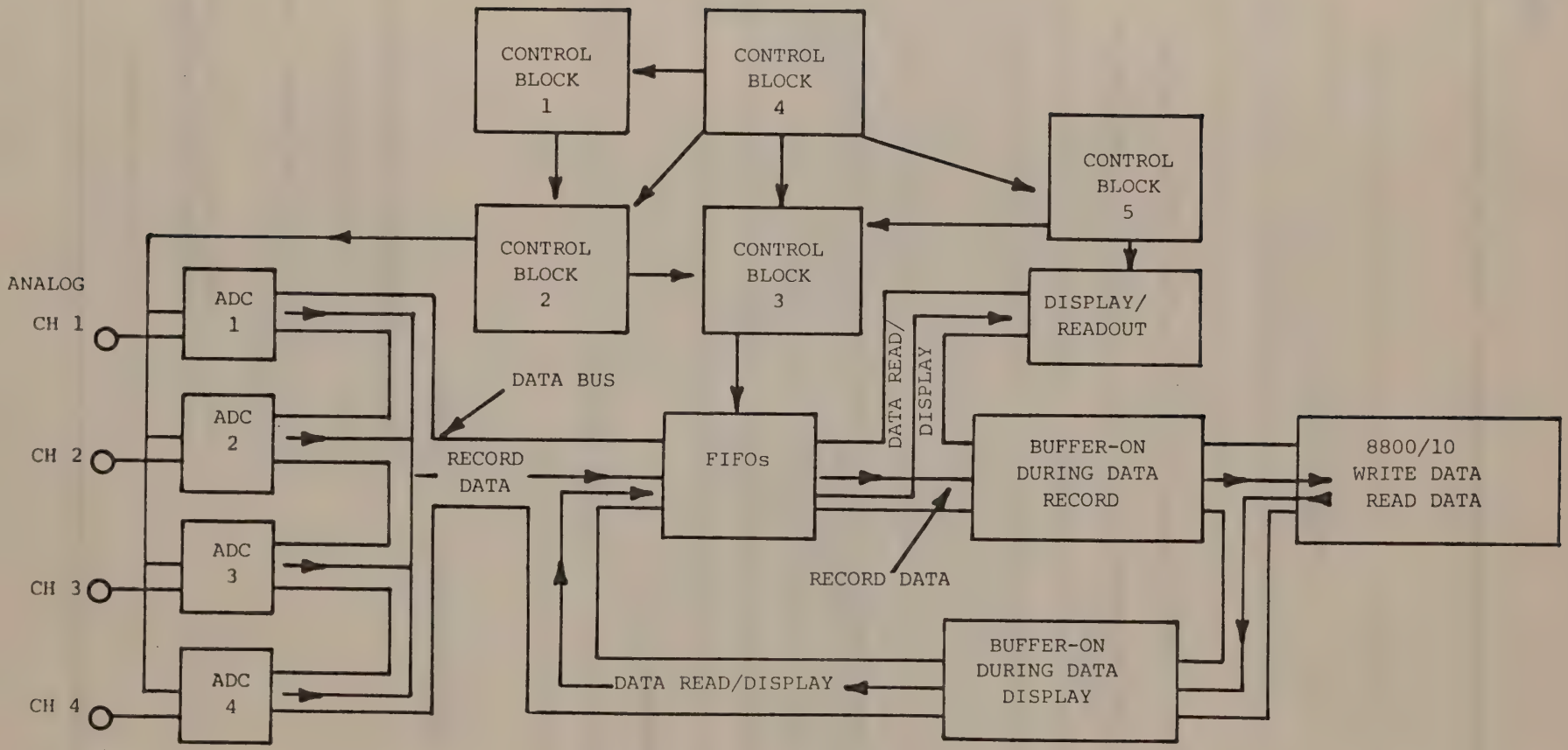
Refer to "Basic Control Diagram"

The 8210-2 digital board controls the flow of data from the four analog to digital converter (ADC) channels to the 8800/10 memory module during data recording. When reading or displaying data the 8210-2 board will read data out of the 8800/10 to the display circuitry or out to the CAMAC interface.

The data bus used (see diagram) is tri-state and allows data to be bussed in both directions. When recording data the ADCs are active, supplying data to the FIFOs which then store data in the 8800/10 module. When reading/displaying data, the ADCs are inactive and data is recirculated from the 8800/10 to the FIFOs and out to the display/readout circuitry.

Control Blocks 1-5 control the flow of data and are described in this manual. Briefly they are:

CONTROL BLOCK #	FUNCTION
1	Master clock control for data recording.
2	Control of data input from ADCs.
3	Controls FIFO input and output, timing, and 8800/10.
4	Control of timing when switching from data record to data readout/display.
5	Control of data display/readout.



8210 - BASIC CONTROL

CONTROL BLOCK 1

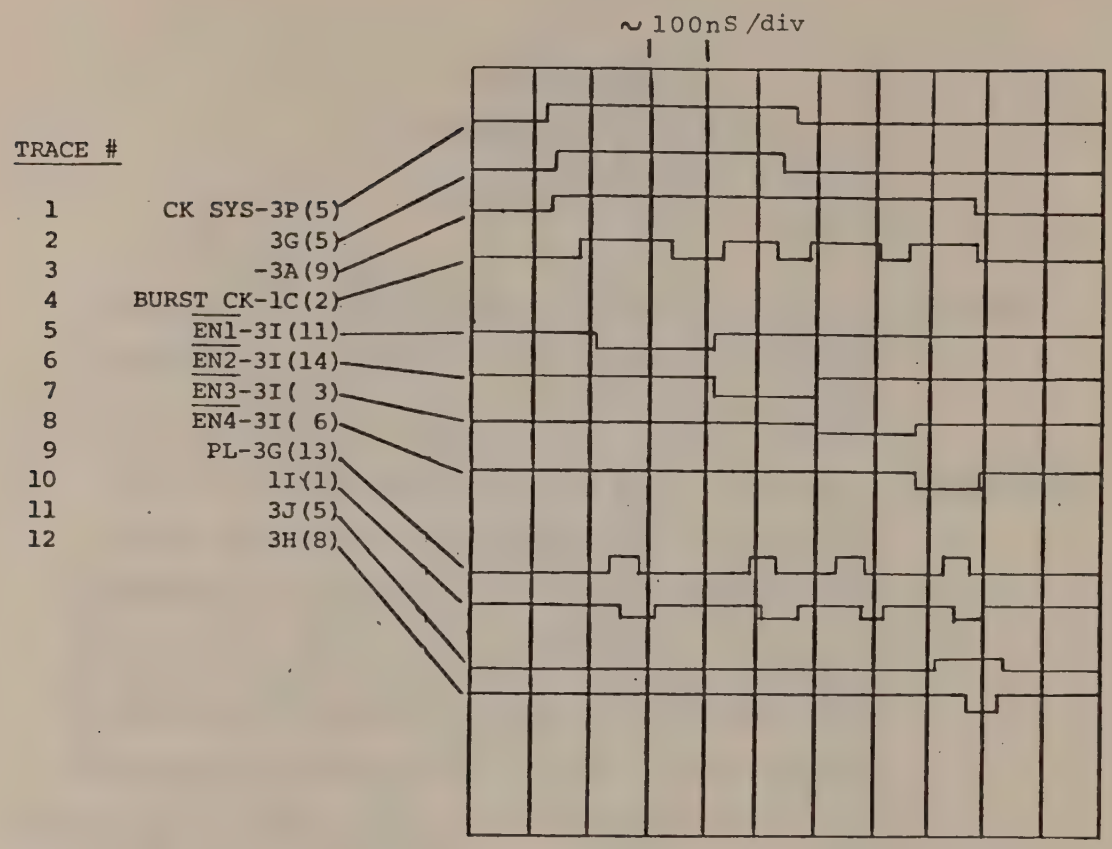
SYSTEM CLOCK GENERATOR

(Refer to Diagram 1)

FUNCTION: Generates - a) Clock for system timing; b) "Hold" and "Start Conv." commands for ADC Boards; c) and triggers Control Block 2 to input data from ADC data storage latches.

DESCRIPTION: A 4MHz crystal osc. (5S) is divided down to 1MHz (4R). This output is fed to other dividers (5R & 3R) and all clocks are then fed to clock multiplexer (3P). Output of 3P (Ck Sys.) is the sampling clock which controls system timing when recording data. The output frequency of 3P depends on the position of the front panel switch which controls 3P(9,10,& 11). The positive edge of 3P(5) triggers 3G (trace 2), a 500nS mono stable, which generates the hold and start convert pulses for the ADC boards. 3G(5) also triggers control block 2 to input data from the ADCs and temporarily store the data in the 9403 FIFOs.

TIMING DIAGRAM FOR CONTROL BLOCKS 1 & 2

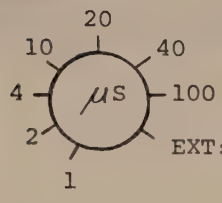


SETUP: 4 Channel sampling mode

1 μsec sampling rate

Scope trigger = Clock out

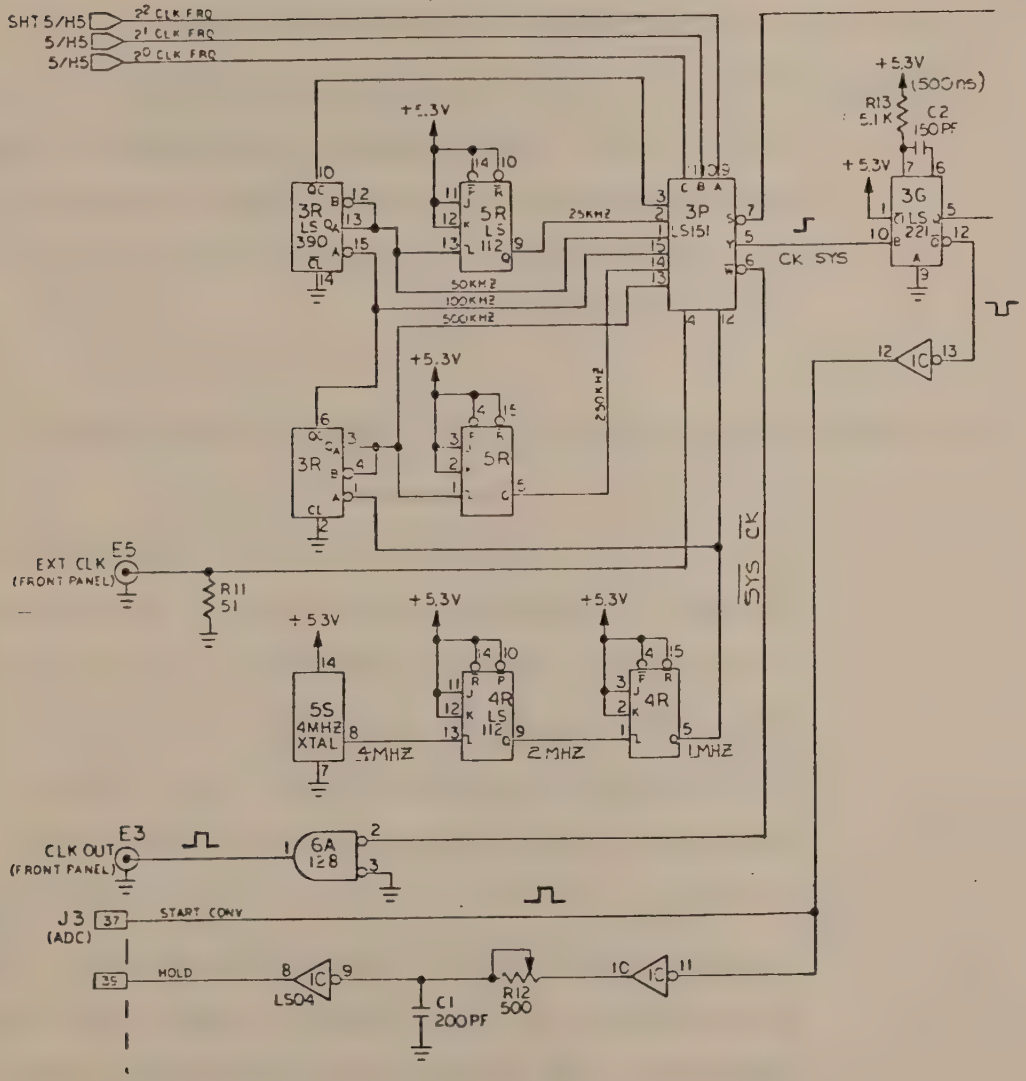
DIAGRAM 1.



EXT: CLOCK INPUT

CONTROL BLOCK 1

SAMPLING INTERVAL FRONT PANEL SWITCH



TO ADC BOARD Int. Cct. 3A (FIG.E)

CONTROL BLOCK 2

STORAGE OF ADC DATA INTO FIFO

(Refer to Diagram 1)

FUNCTION: Control Block 2 is triggered by the positive edge of 3G(5). Once triggered it will fetch data from the ADC storage latches and temporarily store in the 9403 FIFOs. The number of data words fetched depends on the position of the front panel switch "INPUT CHANNELS".

DESCRIPTION: The positive edge of 3G(5), trace 2, triggers 3A(9) to turn on (trace 3). This enables the "Burst Ck", (trace 4) to turn on. The number of pulses in the burst depends on the number of channels selected (1,2 or 4). This is controlled by shift register 3I and multiplexer 3J. As a "1" is shifted through 3I, the "Enable Data" signals to the ADC boards are generated (trace 5,6,7,8). When an "Enable Data" line is low, data from the corresponding ADC storage latch will appear and be loaded into the FIFOs. The shift sequence is terminated by multiplexer (3J) which is controlled by the "INPUT CHANNELS" switch. After 3J(5) goes positive, the sequence will be terminated (traces 11 & 12). Burst Ck also is gated through MUX 1 (3F) to trigger 3G (trace 9). The output of 3G is the parallel load pulse

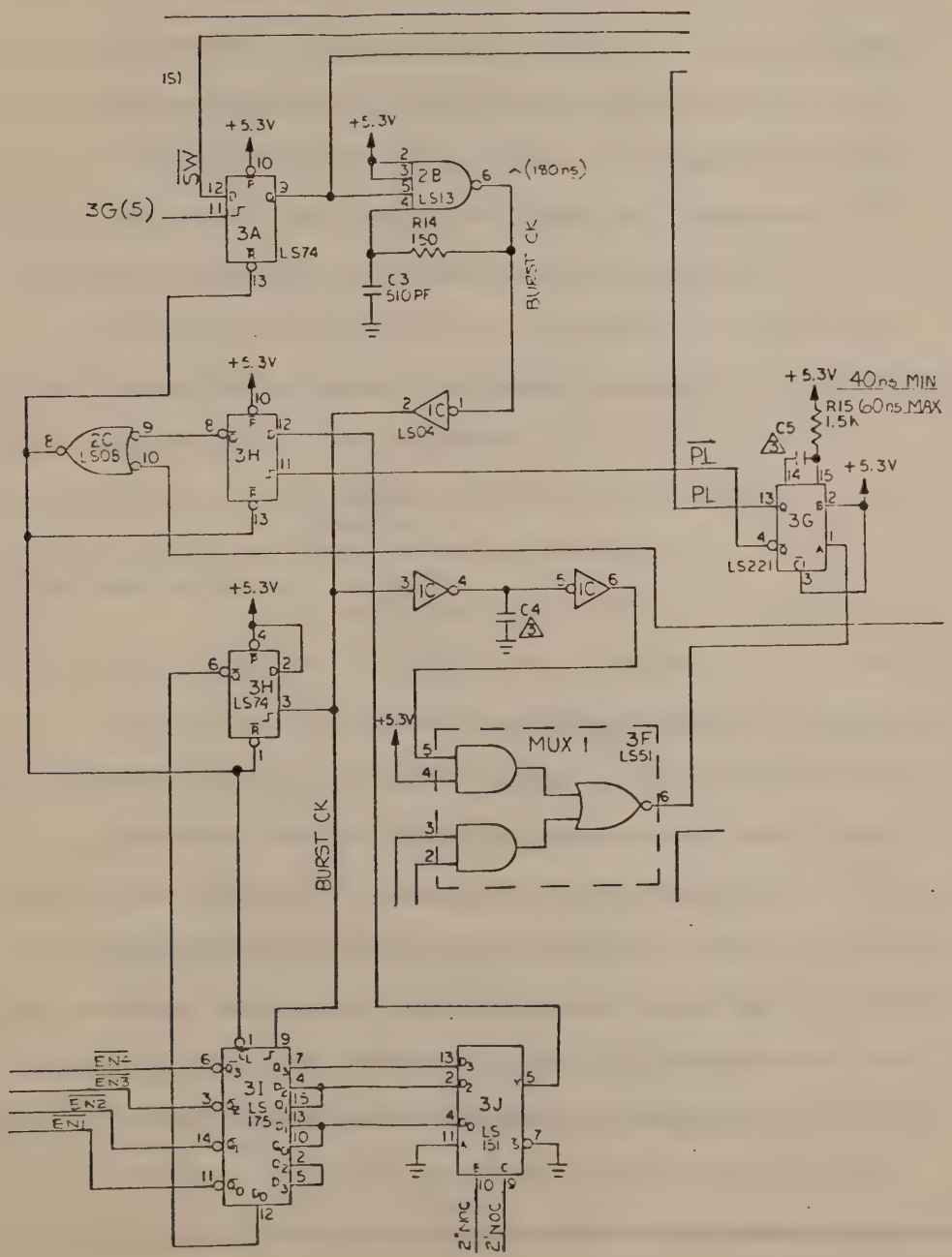
(PL) to the FIFOs which loads the data into the FIFOs. Once a FIFO has accepted data it responds with "INPUT REGISTER FULL", trace 10, which means that no more data can be stored until this signal goes high again. The lower half of MUX 1-3F(3&2) is disabled during the data taking mode. Similarly, the upper half -3F(5) is disabled in the readout & display mode.

POSSIBLE PROBLEMS:

1. The Burst Ck does not terminate its sequence properly and free runs. This may be caused by the period of 2B - "Burst Ck" being too short.

2. In the data taking mode the FIFOs data are always unloaded faster than loaded. This means that $\overline{IRF}$ "INPUT REGISTER FULL" should always be high when PL goes high. If it is not then the FIFO is bad or data is not being unloaded fast enough and the FIFO is overfilling. Overloading of the FIFOs can be detected by noting if all 3 of the $\overline{IRF}$ lines from the 3 FIFOs are low together when a PL is performed.

CONTROL BLOCK 2



CONTROL BLOCK 3

(Refer to diagram 2)

FUNCTION: Control block 3 has two functions; 1.) In the data recording mode it controls the unloading of data from the FIFOs and writing & refreashing of the 8800/10 memory. 2) In the readout and display mode it controls the loading of data into the FIFOs and readout & refreash of the 8800/10.

CONDITIONS: Data recording mode: MUX 1b, 2b, 3b, 4b enabled (chips 3F,3E).

MUX 1a, 2a, 3a, 4a disabled (chips 3F,3E).

Readout & display mode: MUX 1a, 2a, 3a, 4a enabled (chips 3F, 3E)

MUX 1b, 2b, 3b, 4b disabled (chips 3F, 3E)

DESCRIPTION: a) Data Recording Mode:

After data is stored in the FIFOs by PL it bubbles to the top and by lowering the $\overline{\text{ORE}}$ signal (pin 23 of 1I, 1H, 1F) the FIFO indicates that data is available to be removed. These signals propagate through MUX 2b and appear as a TTL low at 3D(12) (Trace1). On the next positive edge of the FIFO Ck (Trace 2), 3D(9) changes state (Trace 3) which generates a $\overline{\text{MEM}}$ $\overline{\text{CK}}$ to the 8800/10 module. On the

positive edge of MEM CK the 8800/10 will store the data appearing at the FIFO outputs. MEM CK also propagates through MUX 3b to generate $\overline{\text{TOP}}$ (transfer out parallel) which transfers the data word out of the FIFO. It should be noted that the purpose of chip 3C(3, 1, 6, 15) is to pulse shape $\overline{\text{MEM}}$ $\overline{\text{CK}}$. $\overline{\text{MEM}}$ $\overline{\text{CK}}$ is turned on by the positive edge of FIFO CK and then turned off by the FIFO CK negative edge via 3C(6). When MEM CK goes high it triggers $\overline{\text{MCIP}}$-3B(12) (Trace 4) which indicates a Memory Cycle in Progress. This signal is used to block refreashing of the 8800/10 memory during a memory read or write cycle. Note-overlap of MEM CK and RFSH will cause invalid data to be read or written in the 8800/10. There must be a minimum of 400ns between positive edges of MEM CK and RFSH.

Every 8 to 10 usecs, Control Block 3 will insert a refresh cycle to refreash the dynamic memory in the 8800/10. When RFSHQ-3B(4), Trace 5, goes high then it is time to do a refresh. Since the FIFOs are always unloaded faster than they are loaded (in the data recording mode) there will be some FIFO CK periods during which there is no data available for storage into the 8800/10. It is only during these times that refreshes are allowed. Note that "RFSH"-3D(6), Trace 8, occurs only when $\overline{\text{MCIP}}$ is not present even though RFSHQ, Trace 5, has been present for many FIFO CK periods. Once a refresh cycle is started $\overline{\text{WDIS}}$ (Write

disable)- 2C(6), is lowered to stop MEM CK from being generated during the refreash (Trace 7).

DATA READOUT & DISPLAY MODE:

In this mode the control block functions as before except that:

1) Data is loaded into the FIFOs from the 8800/10 and unloaded into the DAC display and readout latches.
2) Data is loaded into the FIFOs at a faster rate than it is unloaded. This is because data must be inputted into the DAC display latches at a constant rate in order to prevent display jittering.
3) The MEM CK pulse (which now reads data out of the 8800/10) is triggered by $\overline{\text{IRF}}$ which means there is room to store a word in the FIFOs. MEM CK then triggers PL which in turn actually loads the data.
4) FIFO CK runs at a slower speed (440ns) since the 8800/10 readout speed cannot exceed 400ns/cycle.
5) $\overline{\text{TOP}}$ is generated by the display & readout control block.

POSSIBLE PROBLEMS:

a) If "FIFO CK" is set too fast (210ns) then the 8800 may not have time to complete a memory cycle in the data recording mode.
b) If "FIFO CK" is set too slow (230ns) the FIFOs may not be unloaded fast enough resulting in data overflow in the

data recording mode.

c) In the readout mode, setting FIFO CK faster than 440ns may not give the 8800/10 time to complete the readout cycle. Slower than 500ns may result in display jitter.

NOTE:

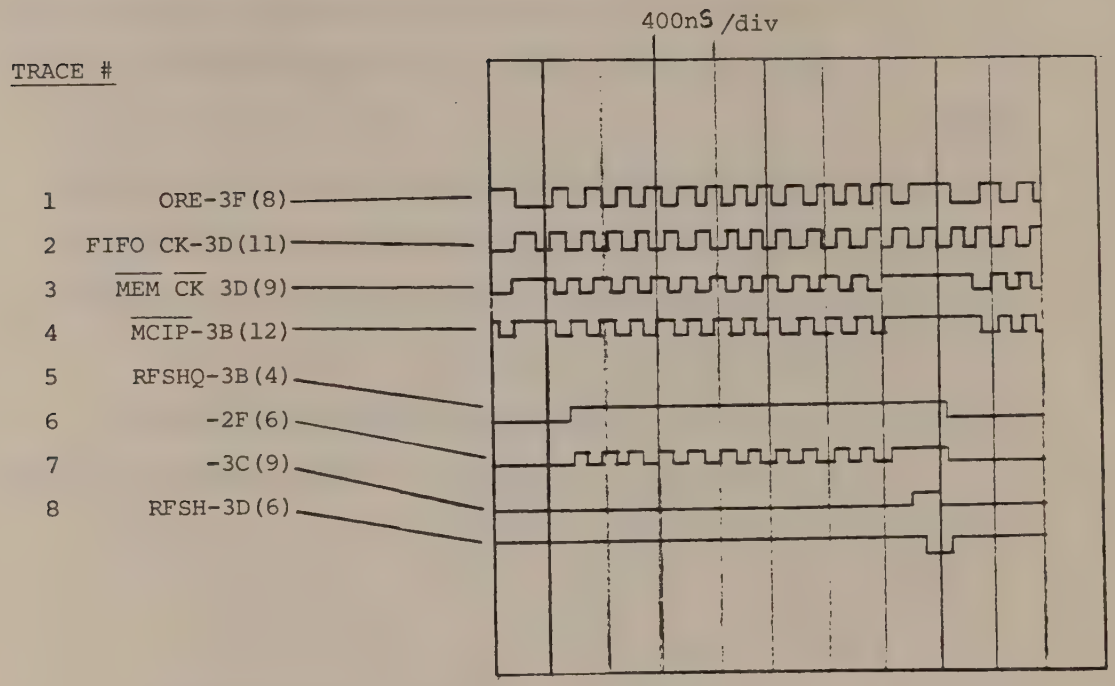
When viewing these signals on a normal scope it will be hard to see the pattern shown on diagram 2 as RFSHQ, ORE & FIFO CK are all asynchronous to one another. For correct operation check that:

1) Monostable and FIFO CK timing is correct.

2) RFSH does not occur during $\overline{\text{MEM}}$ $\overline{\text{CK}}$ and vice versa.

3) Make sure that 3C is a 74S112 & 3D is a 74S74 not 74LS112 or 74LS74.

TIMING DIAGRAM FOR CONTROL BLOCK 3

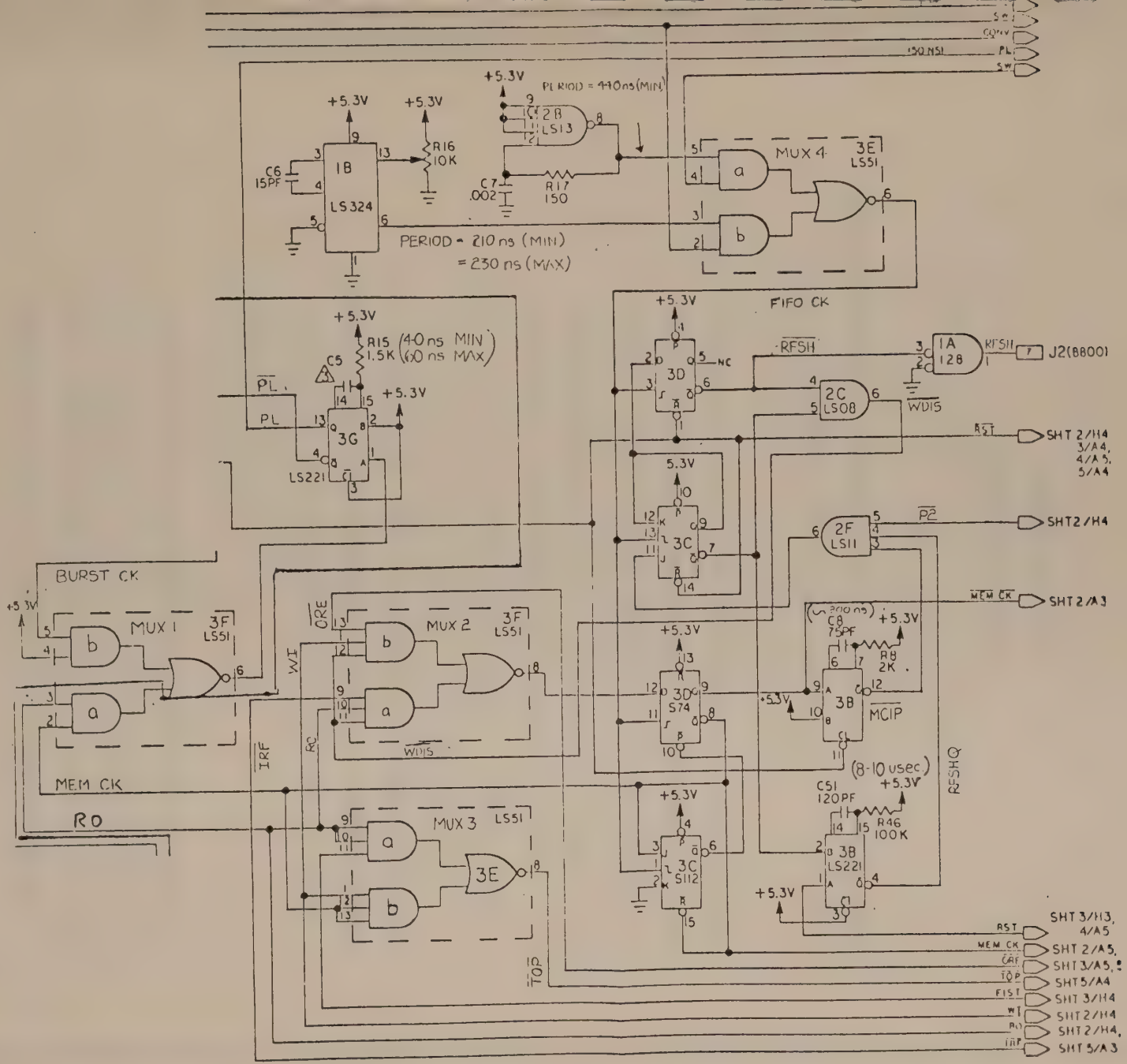


SETUP: 4 Channel mode

1 μsec sample rate

Data recording mode

DIAGRAM 2.



CONTROL BLOCK 3
10.13

CONTROL BLOCK 4

SWITCH OVER TIMING

(Refer to diagram 4 and sheet 2 of schematic)

FUNCTION: Controls the switching of control functions from the data recording mode to the readout & display mode.

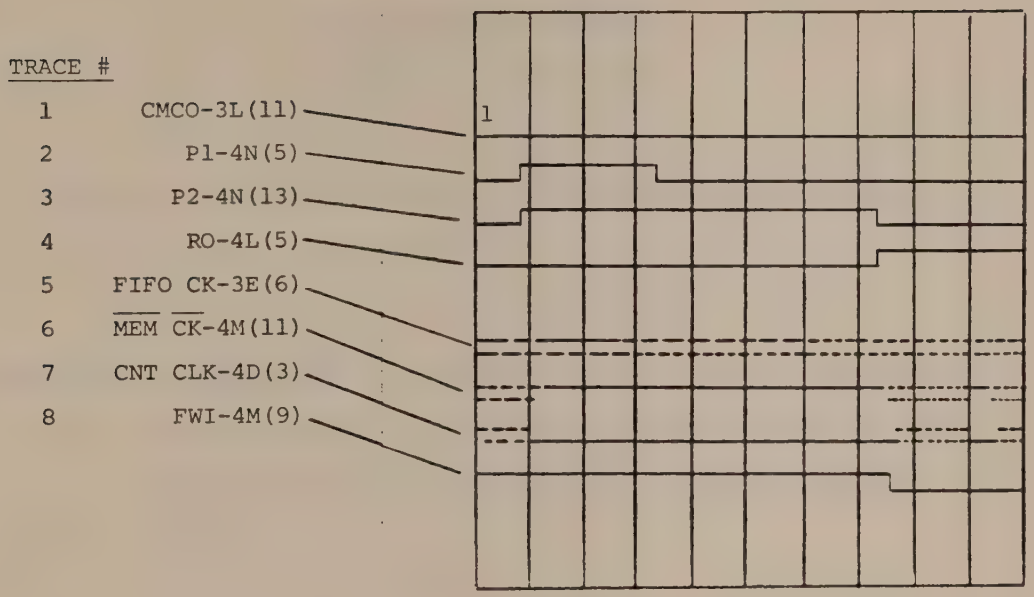
DESCRIPTION: Counters 3N, 2N, 2M, & 3M perform two functions. In data record mode they count the number of post-trigger samples and then trigger the logic to switch from data record to the readout/display mode. In the readout/display mode they count the number of words read out of the 8800/10. At the beginning of each 8800/10 readout scan they trigger FWI (First Word In) into the FIFOs. FWI indicates that the data word being loaded into the FIFOs corresponds to the earliest sample digitized in Channel 1. After FWI emerges from the FIFOs (now called FWO-First Word Out) it initializes the readout/display circuitry.

After the post-trigger samples have been performed CNCO-3L(11), Trace 1, is generated. This triggers PL (Trace 2) which triggers P2 (Trace 3). P1 and P2 are used to create pauses between the data recording mode and the display/

readout mode. These pauses are necessary to allow a clean change of control functions. P1 must be at least 10 usec longer than P1. During P1 and P2 all multiplexing logic is switched and the 8800/10 is changed from the write-in to the readout state.

NOTE: This sequence is most easily seen by issuing $\overline{F(9)s}$ at a 10 cycles/sec rate; pull pin 5M(2) out of the socket and jumper connect to pin 2C(2). This will cause the 8210 to go into the display mode after the 8800/10 fills memory once. The front panel LED will be flickering on and off at 10hz/sec. Trigger scope on 3L(11) to see the sequence.

TIMING DIAGRAM FOR CONTROL BLOCK 4



SETUP: 4 Channel Mode

1 μsec Sample Rate

DIAGRAM 4.

CONTROL BLOCK 5

DISPLAY/READOUT CONTROL

(Refer to Diagram 5)

FUNCTION: To decode the 8800/10 data for output to the display generator or CAMAC readout.

DESCRIPTION: Display Mode (in this mode 4H (6) is always TTL high and 5G(all), 4G(11,12,13), 4F(1,2,3), and 5H(9,11,12) are inactive - these I.C.s. are only active during CAMAC readout.

The data decode circuitry is activated by a low transition of 4P(3) (Tracel). This indicates that data is ready to be outputted from the FIFOs. The first data word to come out of the FIFOs corresponds to the earliest sample digitized in channel 1 and is flagged by FWO (First Word Out), Trace 3 being high. When 4P(3) goes low it triggers 6R(13), Trace 2,and this is gated with FWO at 4F(11), Trace 4. This signal, in turn, activates flop 5H(5&6). The purpose of this circuitry is to scan the correct number of channels and then latch the proper data into the display latches (1L & 2K). Assume that the front panel display switch is

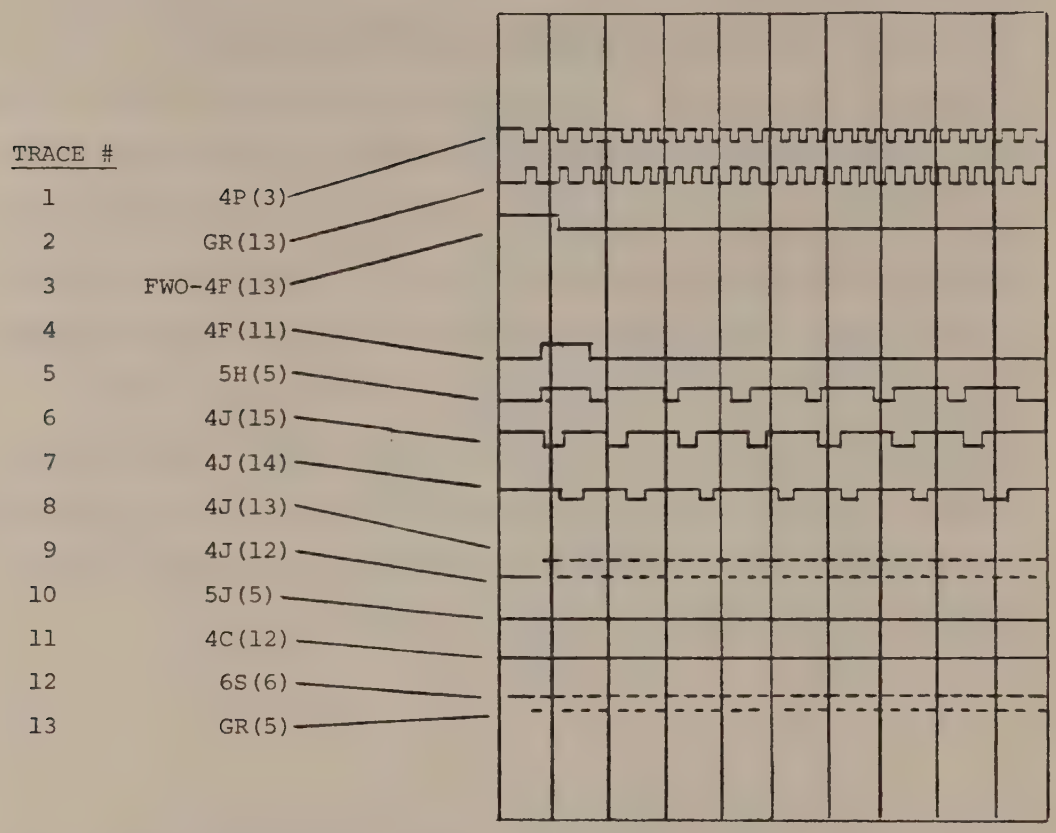
set to channel 3 (number of channels = 4). The data coming out of the 8800/10 will look like:

CH 1	SAMPLE 1	(FWO)
2	"	1
3	"	1
4	"	1
1	"	2
2	"	2
3	"	2
4	"	2
1	"	3
.	.	.
.	.	.
.	.	.

The decode circuitry must first scan through CH1, sample 1 and CH2, sample 1, and then latch CH3, sample 1 into the display latches. From this point on channels 4, 1 and 2 are rapidly scanned and then CH. 3 data latched again. That is, on the first pass 2 data words are discarded and the third latched, from then on 3 data words are discarded and the fourth latched. The circuitry works in a similar fashion for displaying other channels. The circuitry which determines when to latch the proper data is composed of 5H, 5K, 4J and 5J. I.C., 5K is a tri-state buffer which is connected to the front panel switches. When 5H(5) goes high, it activates 5K(4 & 1) which places the "Display

Channels" switch position on 5J(1 & 11). 5J is a multiplexer which selects one of four inputs which are sequentially lowered from 4J. When 4J(15) is low, it indicates that the data being output from the FIFOs is from CH 1. Similarly 4J(14) indicates CH 2 data and so on (Traces 6,7,8 & 9). When displaying CH 3, the output of 5J(5) (Trace 10) will go low as soon as 4J(13) goes low indicating that CH 3, sample 1 data is ready to be latched. This signal then propogates through 4C(12) to become the latch pulse. Note that the output of 4F(8) resets 4J and 5H. This enables 5K(10 & 13) to place the "Input Channels" switch position on 5J. From now on 4J will scan through to 4J(12) (Trace 9) and generate latch pulses. This now latches in every fourth data word. Data is removed from the FIFOs when GR(5) triggers (Trace 13).

TIMING DIAGRAM FOR CONTROL BLOCK 5



CONDITIONS: Display mode

4 Channel/1 μsec Sampling Rate

Displaying Ch. 3

DIAGRAM 5.

APPENDIX A

This appendix describes some common post-trigger sample control configurations for LeCroy/CA Models 8212, 8210, and 2264.

The number of PTS taken after receipt of the stop trigger is controlled by programming a 16 bit binary number. For Models 8210 and 2264, 3 bits of the number are controlled by the front panel switch, the remaining 13 are set by jumper options. The 8212 is similar except the 3 bits are set via a CAMAC command. Figures 1-3 show the PTS scaler configurations for the different models. These are four bit scalers. Before receipt of the stop trigger, the 16 bit data word is loaded into the counters. Afterwards, the counters count up until the appropriate overflow is detected.

The number of PTS is independent of the number of channels selected. There is, however the constraint that the maximum PTS is one-half of the memory size. (Memory size equals 32K* (number of memory modules)).

To program the correct number of PTS the user must configure the correct jumpers on the PTS header. To do this, find the PTS table you wish to use, then program the header as the table defines it. A "1" state is defined as +5.3 volts; a "0" state as GND. The "PTS CONTROL" bits must be jumpered to the correct pins as defined in the table. As example:

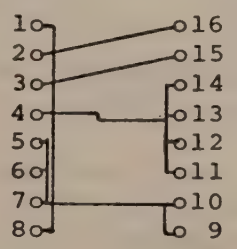
Model #: 8212

Number of Memories: 2 (64K words)

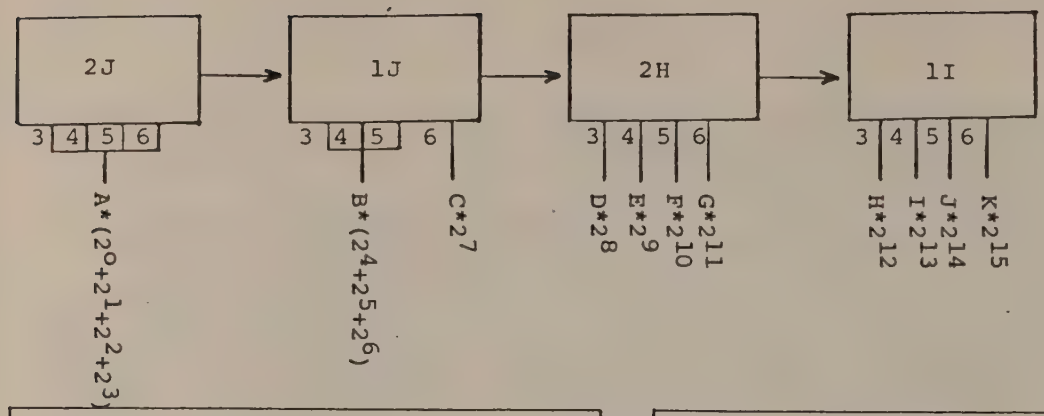
Number of Active Channels: 32 (2K words/channel)

Desired post-trigger sample range: 256 to 2048.

Use Table 3 with J=1. Then header is configured as:



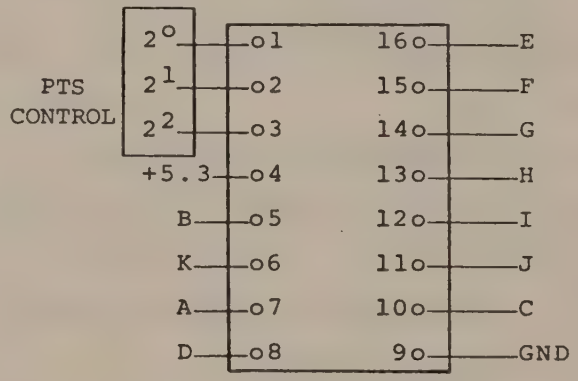
8212 PTS CONFIGURATION



A,B,C,D,E,F,G,H,I,J,K = 0 OR 1

J&K = 0 FOR 1 MEMORY MODULE
K = 0 FOR 2 MEMORY MODULES

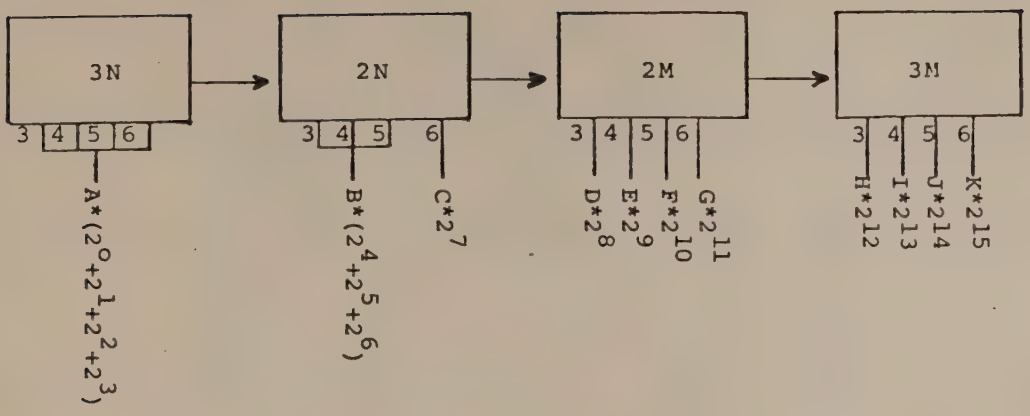
HEADER CONFIGURATION
(SOCKET 1H)



(AS VIEWED FROM COMPONENT SIDE)

FIGURE 1

8210 PTS CONFIGURATION



A, B, C, D, E = 1 F, G, H, I, J, K = 0 or 1

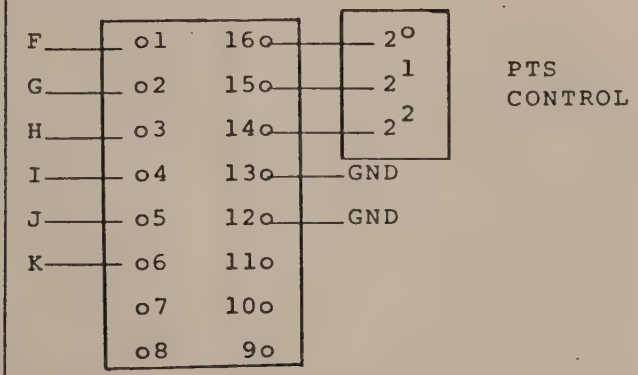
J&K = 0 FOR 1 MEMORY MODULE K = 0 FOR 2 MEMORY MODULES

PTS CONTROL

$(2^2\ 2^1\ 2^0)$	FRONT PANEL SWITCH SETTING
0 0 0	7
0 0 1	6
0 1 0	5
0 1 1	4
1 0 0	3
1 0 1	2
1 1 0	1
1 1 1	0

HEADER CONFIGURATION *

(SOCKET 3L)



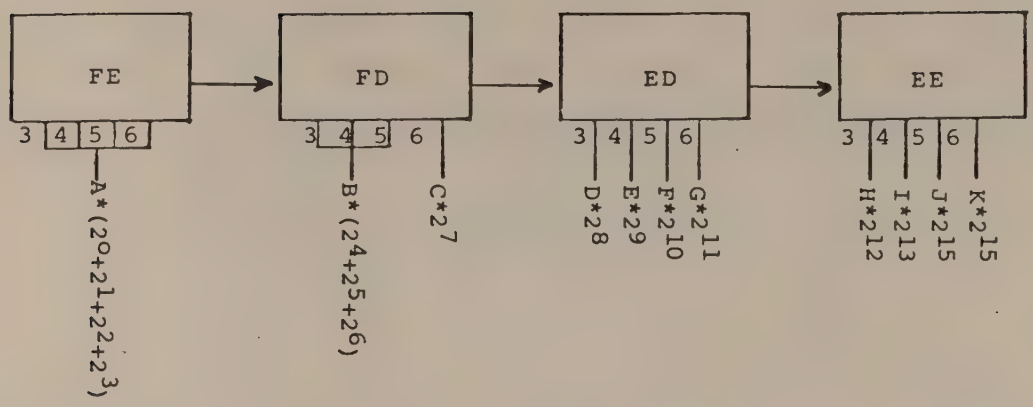
(AS VIEWED FROM COMPONENT SIDE)

*NOTES: 1) A "1" is programmed for F,G,H,I,J or K by not installing a jumper. A "0" is programmed by jumpering to gnd.

2) Connect 10 to 11 for one memory module (32K) or 9 to 11 for two memory modules.

FIGURE 2

2264 PTS CONFIGURATION



A, B, C, D, E, = 0
F, G, H, I, J, K = 0 or 1

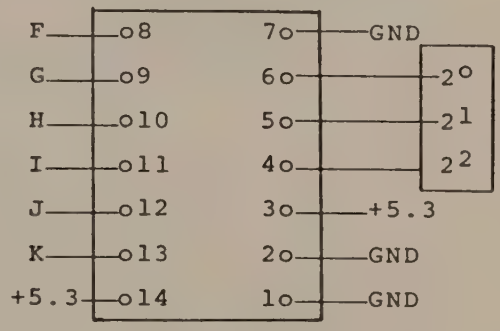
J&K = 0 FOR 1 MEMORY MODULE
K=0 FOR 2 MEMORY MODULES

PTS CONTROL

$(2^2\ 2^1\ 2^0)$	FRONT PANEL SWITCH SETTING
0 0 0	8
0 0 1	7
0 1 0	6
0 1 1	5
1 0 0	4
1 0 1	3
1 1 0	2
1 1 1	1

HEADER CONFIGURATION

(SOCKET A0)



(as viewed from component side)

FIGURE 3

(ONE MEMORY - J&K = 0)*

1.

K	J	I	H	G	F	PTS CONTROL 2^2	2^1	2^0	B	A	PTS
0	0	1	1	1	1	0	0	0	0	0	1024
						0	0	1			896
						0	1	0			768
						0	1	1			640
						1	0	0			512
						1	0	1			384
						1	1	0			256
						1	1	1			128

2.

K	J	I	H	G	F	PTS CONTROL 2^2	2^1	2^0	B	A	PTS
0	0	1	1	1	1	0	0	0	1	1	897
						0	0	1			769
						0	1	0			641
						0	1	1			513
						1	0	0			385
						1	0	1			257
						1	1	0			129
						1	1	1			1

3.

K	J	I	H	G	F	PTS CONTROL 2^2	2^1	2^0	C	B	A	PTS
0	0	1	1	1	0	0	0	0	0	0	2048
					0	0	1				1792
					0	1	0				1536
					0	1	1				1280
					1	0	0				1024
					1	0	1				768
					1	1	0				512
					1	1	1				256

4.

K	J	I	H	G	F	PTS CONTROL 2^2	2^1	2^0	C	B	A	PTS
0	0	1	1	1	0	0	0	0	1	1	1793
					0	0	1				1537
					0	1	0				1281
					0	1	1				1025
					1	0	0				769
					1	0	1				513
					1	1	0				257
					1	1	1				1

5.

K	J	I	H	G	F	E	PTS CONTROL 2^2	2^1	2^0	D	C	B	A	PTS
0	0	1	1	0	0	0	0	0	0	4096
				0	0	1								3584
				0	1	0								3072
				0	1	1								2560
				1	0	0								2048
				1	0	1								1536
				1	1	0								1024
				1	1	1								512

6.

K	J	I	H	G	F	E	PTS CONTROL 2^2	2^1	2^0	D	C	B	A	PTS
0	0	1	1	0	0	0	1	1	1	3585
				0	0	1								3073
				0	1	0								2561
				0	1	1								2049
				1	0	0								1537
				1	0	1								1025
				1	1	0								513
				1	1	1								1

*FOR TWO MEMORIES, SET J=1, FOR SAME PTS AS SHOWN IN TABLES
FOR FOUR MEMORIES, SET J&K=1, FOR SAME PTS AS SHOWN IN TABLES

PTS TABLE

(ONE MEMORY - J&K=0)*

7.

			PTS CONTROL 2^2 2^1 2^0												
K	J	I	H	G	F	E	D	C	B	A	PTS				
0	0	1	0	0	0	0	0	0	0	0	8	1	9	2
			0	0	1						7	1	6	8
			0	1	0						6	1	4	4
			0	1	1						5	1	2	0
			1	0	0						4	0	9	6
			1	0	1						3	0	7	2
			1	1	0						2	0	4	8
			1	1	1						1	0	2	4

8.

			PTS CONTROL 2^2 2^1 2^0												
K	J	I	H	G	F	E	D	C	B	A	PTS				
0	0	1	0	0	0	1	1	1	1	1	7	1	6	9
			0	0	1						6	1	4	5
			0	1	0						5	1	2	1
			0	1	1						4	0	9	7
			1	0	0						3	0	7	3
			1	0	1						2	0	4	9
			1	1	0						1	0	2	5
			1	1	1									1

9.

		PTS CONTROL 2^2 2^1 2^0												
K	J	I	H	G	F	E	D	C	B	A	P	T	S	
0	0	0	0	0	0	0	0	0	0	0	1	6	3	8	4
		0	0	1							1	4	3	3	6
		0	1	0							1	2	2	8	8
		0	1	1							1	0	2	4	0
		1	0	0								8	1	9	2
		1	0	1								6	1	4	4
		1	1	0								4	0	9	6
		1	1	1								2	0	4	8

10.

		PTS CONTROL 2^2 2^1 2^0												
K	J	I	H	G	F	E	D	C	B	A	P	T	S	
0	0	0	0	0	1	1	1	1	1	1	1	4	3	3	7
		0	0	1							1	2	2	8	9
		0	1	0							1	0	2	4	1
		0	1	1								8	1	9	3
		1	0	0								6	1	4	5
		1	0	1								4	0	9	7
		1	1	0								2	0	4	1
		1	1	1											1

* FOR TWO MEMORIES, SET J=1, FOR SAME PTS AS SHOWN IN TABLES

FOR FOUR MEMORIES, SET J&K=1, FOR SAME PTS AS SHOWN IN TABLES

PTS TABLES
(TWO MEMORIES - K=0)*

PTS CONTROL $2^2 2^1 2^0$															
K	J	I	H	G	F	E	D	C	B	A		P	T	S	
0	0	0	0	0	0	0	0	0	0	0	3	2	7	6	8
	0	0	1								2	8	6	7	2
	0	1	0								2	4	5	7	6
	0	1	1								2	0	4	8	0
	1	0	0								1	6	3	8	4
	1	0	1								1	2	2	8	8
	1	1	0									8	1	9	2
	1	1	1									4	0	9	6

12.

PTS CONTROL $2^2 2^1 2^0$															
K	J	I	H	G	F	E	D	C	B	A		P	T	S	
0	0	0	0	1	1	1	1	1	1	1	2	8	6	7	3
	0	0	1								2	4	5	7	7
	0	1	0								2	0	4	8	1
	0	1	1								1	6	3	8	5
	1	0	0								1	2	2	8	9
	1	0	1									8	1	9	3
	1	1	0									4	0	9	7
	1	1	1												1

PTS TABLES
(FOUR MEMORIES)

PTS CONTROL $2^2 2^1 2^0$															
K	J	I	H	G	F	E	D	C	B	A		P	T	S	
0	0	0	0	0	0	0	0	0	0	0	6	5	5	3	6
0	0	1									5	7	3	4	4
0	1	0									4	9	1	5	2
0	1	1									4	0	9	6	0
1	0	0									3	2	7	6	8
1	0	1									2	4	5	7	6
1	1	0									1	6	3	8	4
1	1	1										8	1	9	2

14.

PTS CONTROL $2^2 2^1 2^0$															
K	J	I	H	G	F	E	D	C	B	A		P	T	S	
0	0	0	0	1	1	1	1	1	1	1	5	7	3	4	5
0	0	1									4	9	1	5	3
0	1	0									4	0	9	6	1
0	1	1									3	2	7	6	4
1	0	0									2	4	5	7	7
1	0	1									1	6	3	8	5
1	1	0										8	1	9	3
1	1	1													1

* FOR FOUR MEMORIES, SET K=1 FOR SAME PTS AS SHOWN IN TABLES

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